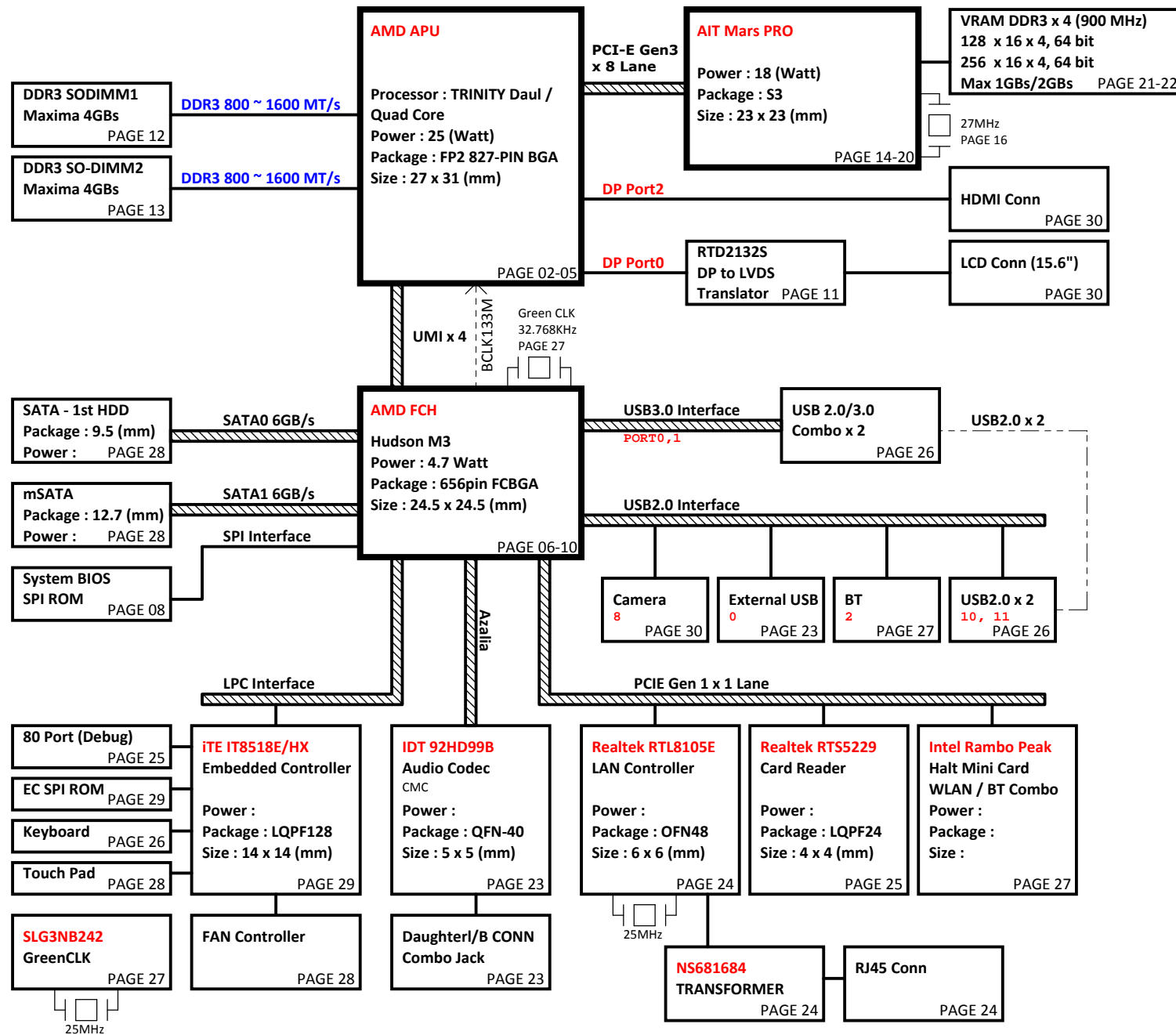


Tiguan1.0_AMD Comal DIS/UMA (15.6") Ultra/Slim

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24728
System Charge Power (+BATCHG)

G5934RZ1U
System Discharge Power
(+1.5V/+3V/+5V)
(+3VSUSV/+3VLAVCC/+1.1V)

Richtek RT8223PZ
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

SL6277/RT8228AZ/AP3407A/ISL6208BCRZ
Processor Power (+VCC_CORE/
+1.2V/+2.5V/+VDDNB_CORE)

Richtek RT8207L
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

Richtek RT8228AZ
PCH Power (+1.1VS5)

RT8152E/G5193/G5193R41U/NB650
DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/
+1.5V_VGA/+1.8V_VGA/+VDDCI)



PROJECT : U56
Quanta Computer Inc.

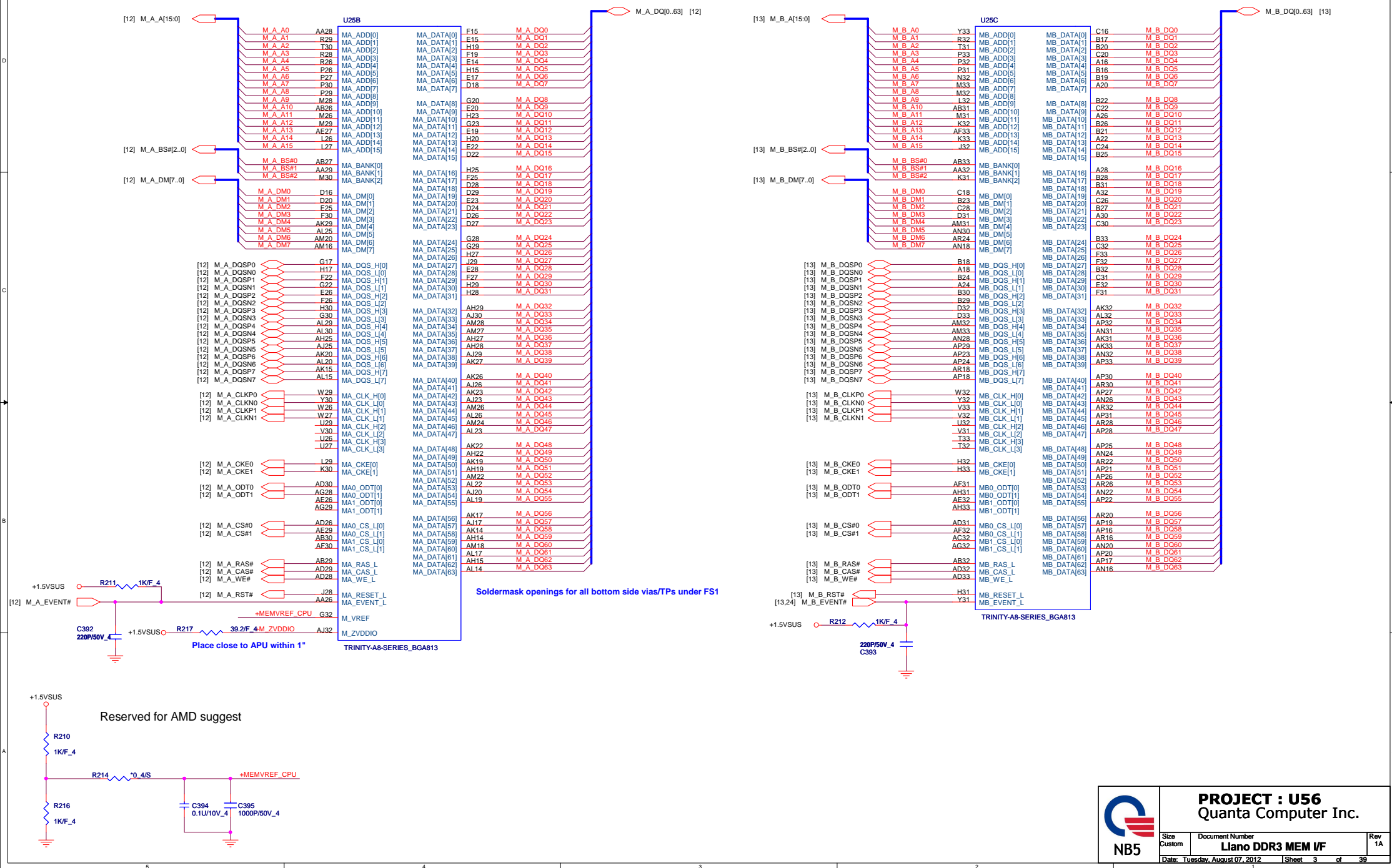
Size A3	Document Number Block Diagram	Rev 1A
Date: Thursday, August 09, 2012	Sheet	1 of 39



8



1A



Place caps with APU < 1 inch
route PCIe as 85ohm +/- 10%

DP0 output to
eDP to LVDS converter

Display port power 1.5V min 1.2v max : 1.65v

4/19 HDMI change to DP2 for Comal.

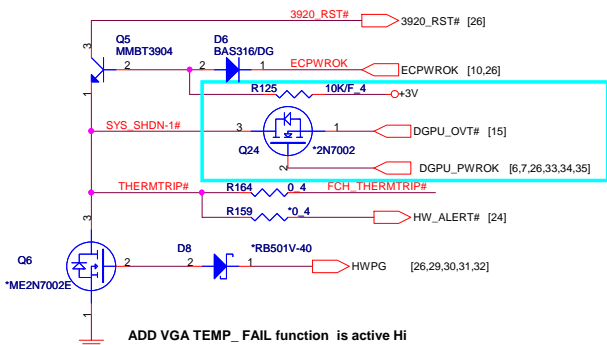
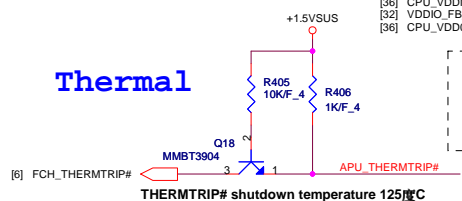
DP2 output to
HDMI connector

note --HDMI P&N can not swap

Note: CLK_APU_HCLKP/N is 100MHZ SSC

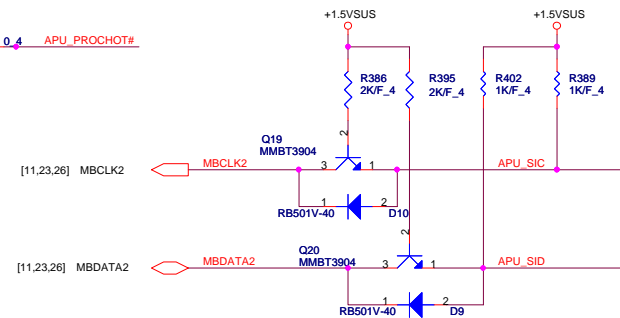
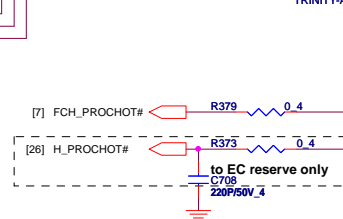
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

Thermal



over 120 degree C= Low

When 100K-NTC 100 C=6.164K
Thermal Trip = 120 C

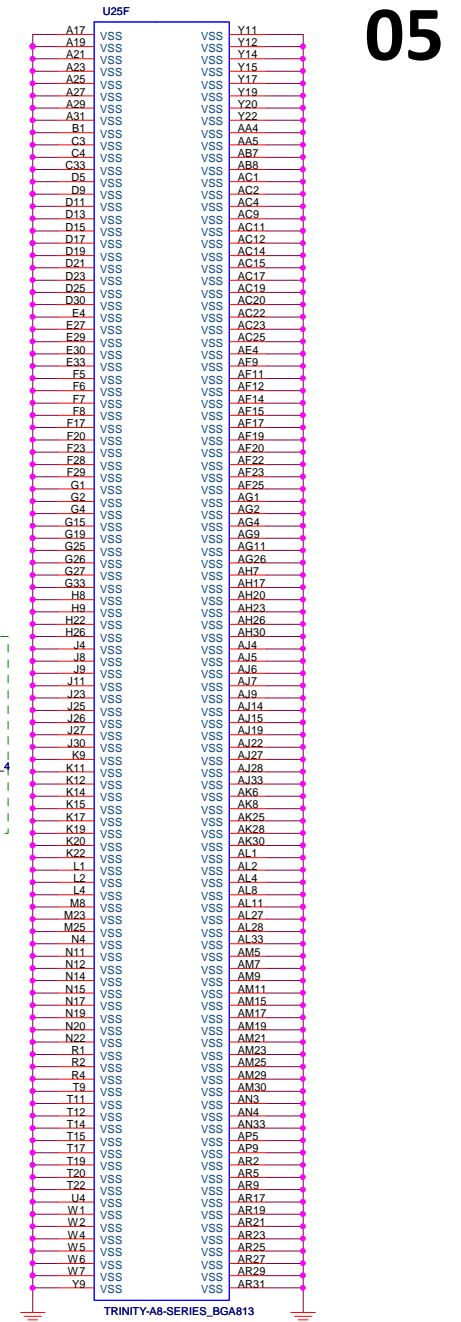
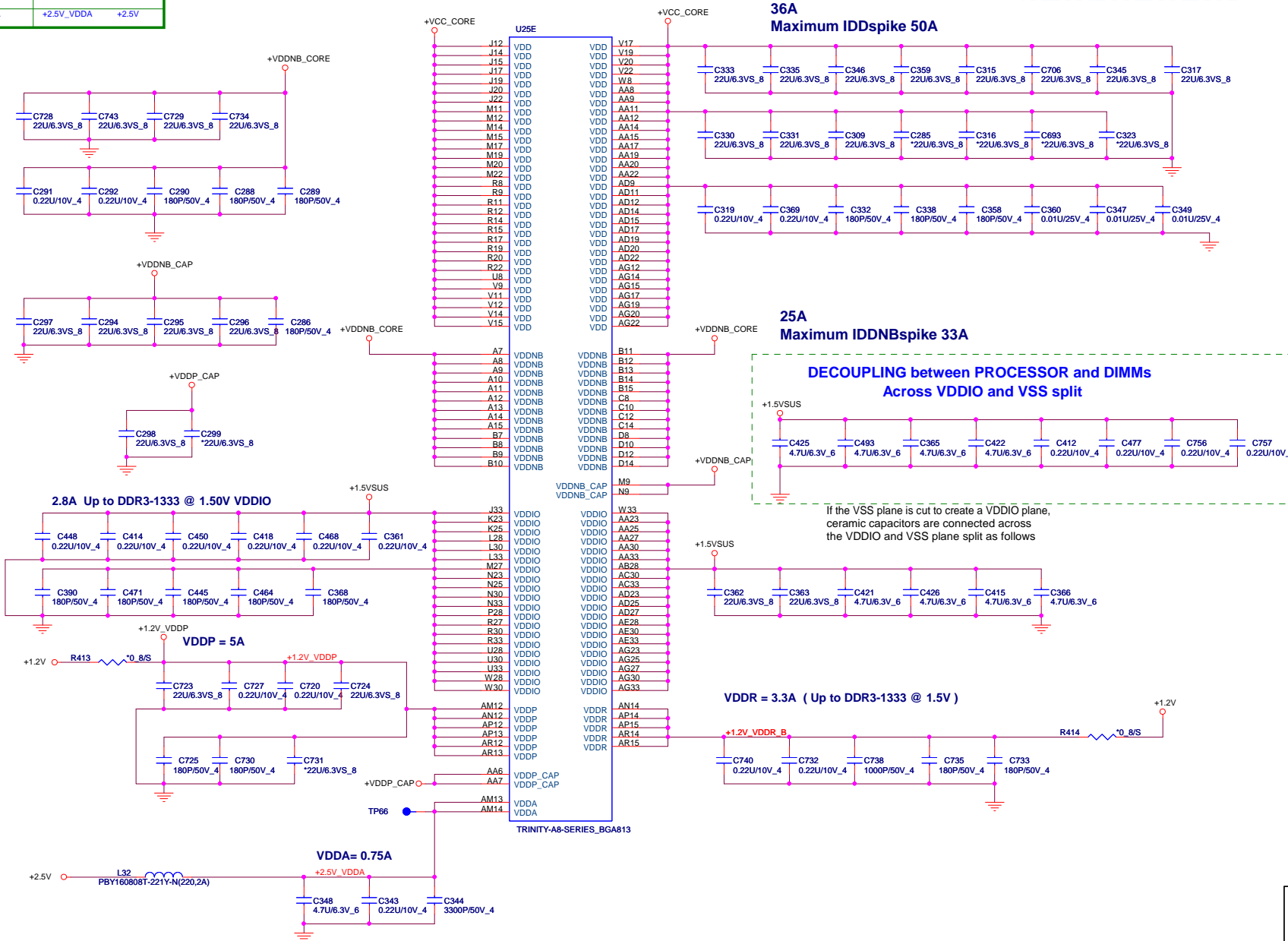
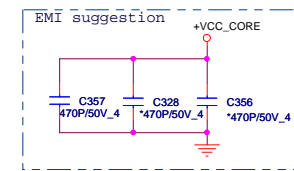


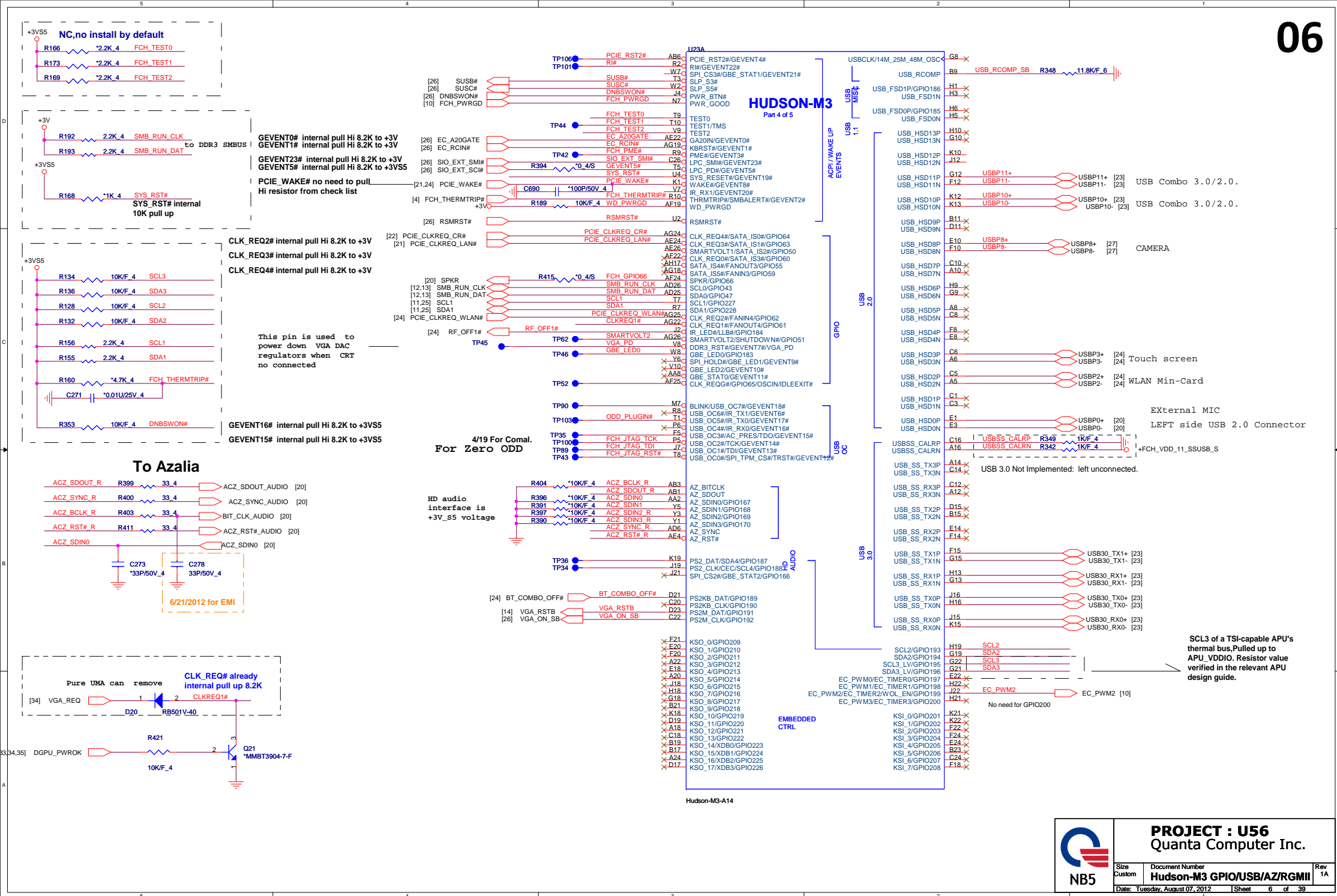
PROJECT : U56
Quanta Computer Inc.

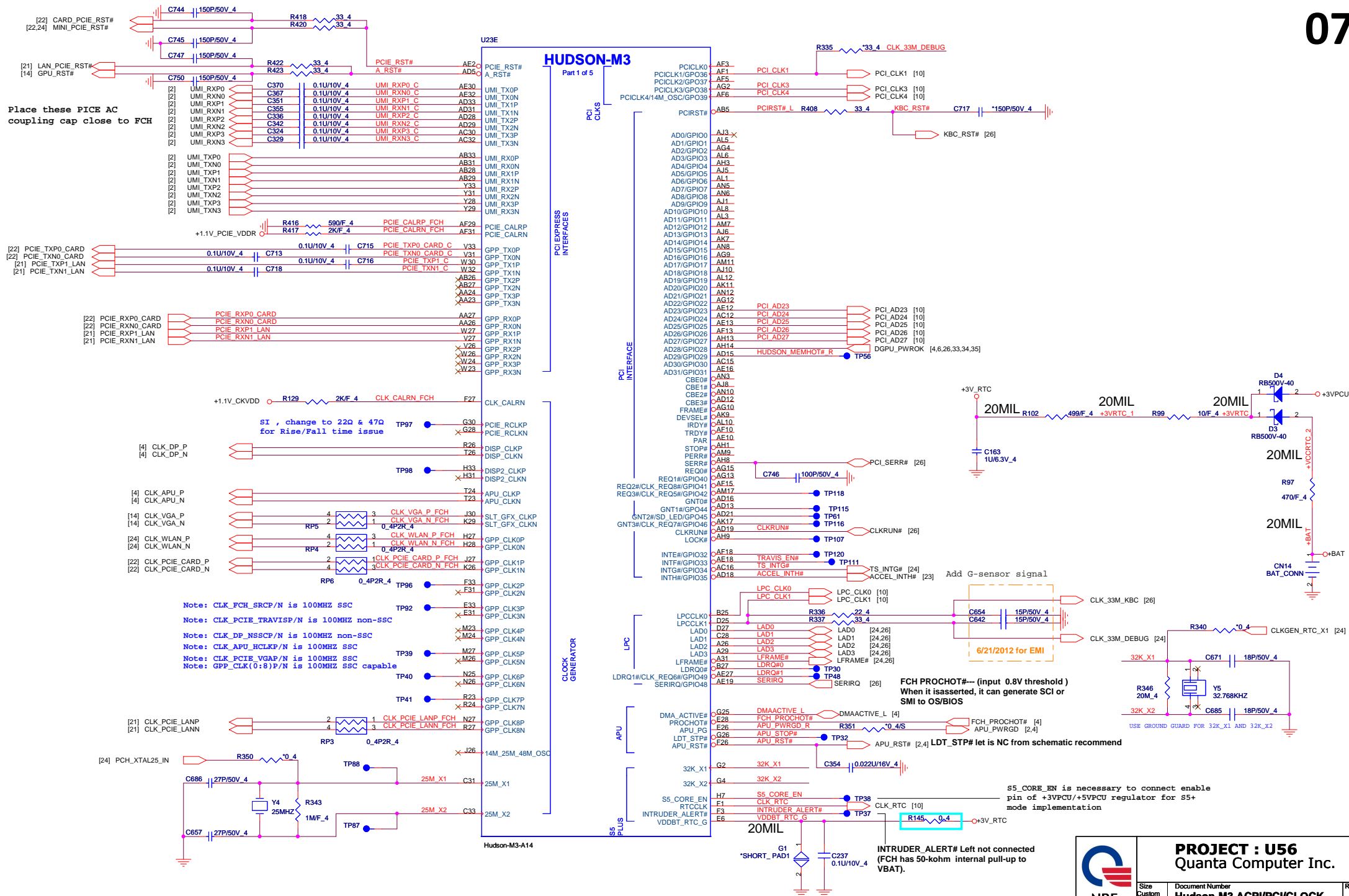
Size	Document Number	Rev
	Llano Display/Misc	1A
Date:	Tuesday, August 07, 2012	Sheet 4 of 39

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



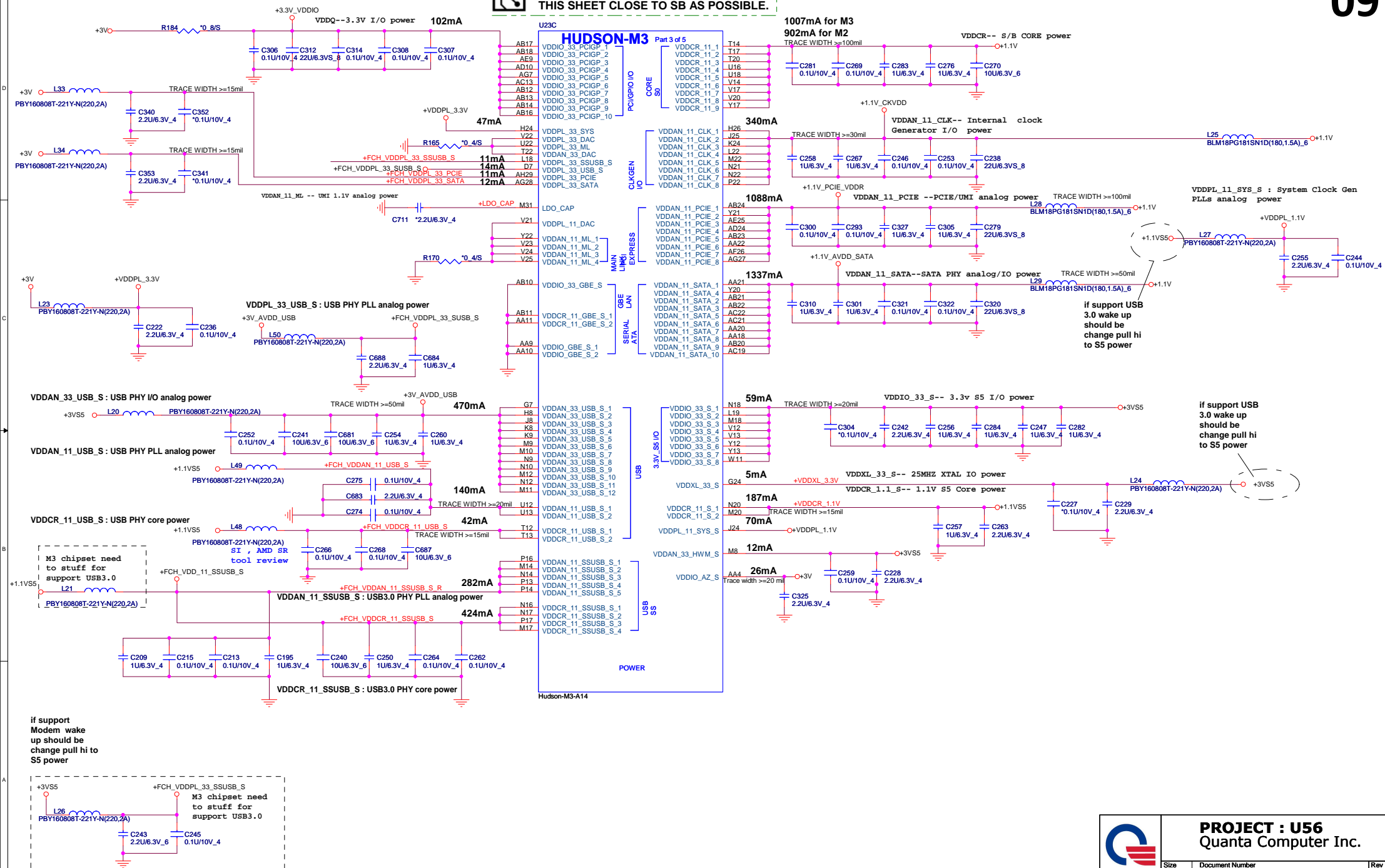






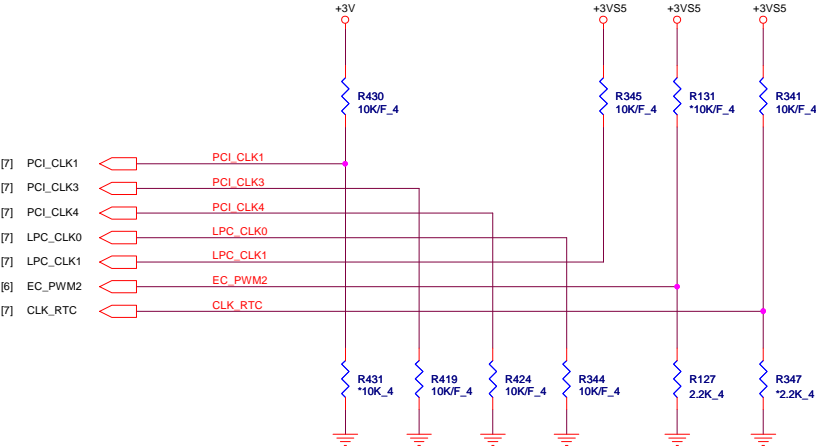


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

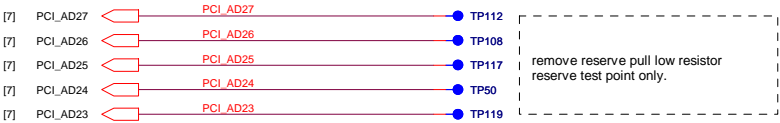


REQUIRED STRAPS

		PCI_CLK1		PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

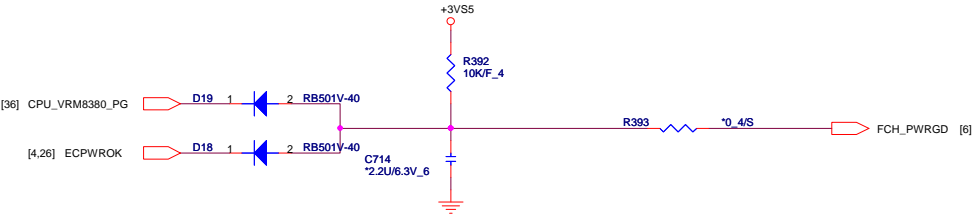
DEBUG STRAPS

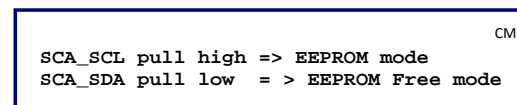
FCH has 15K Internal Pull Up for PCI_AD[27:23]



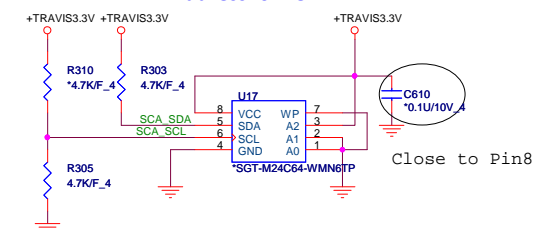
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH_PWRGD

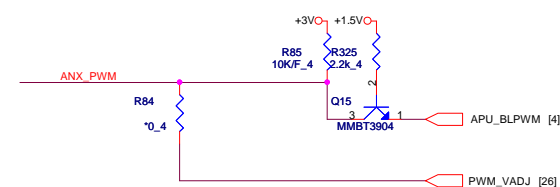




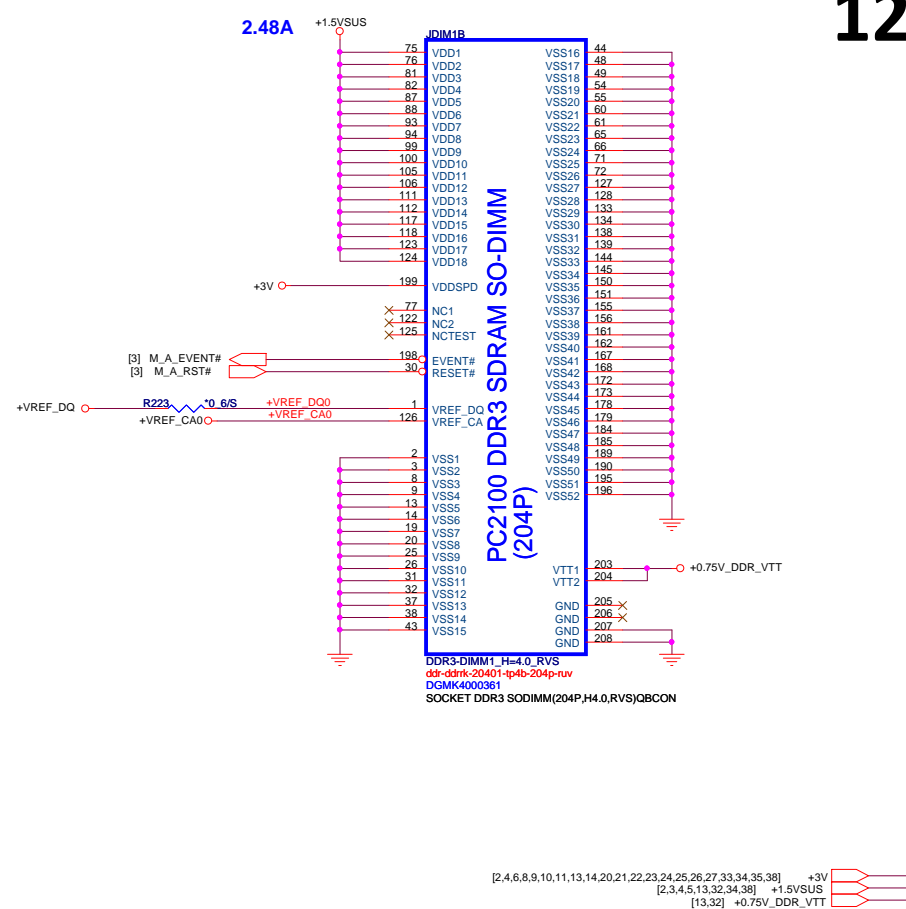
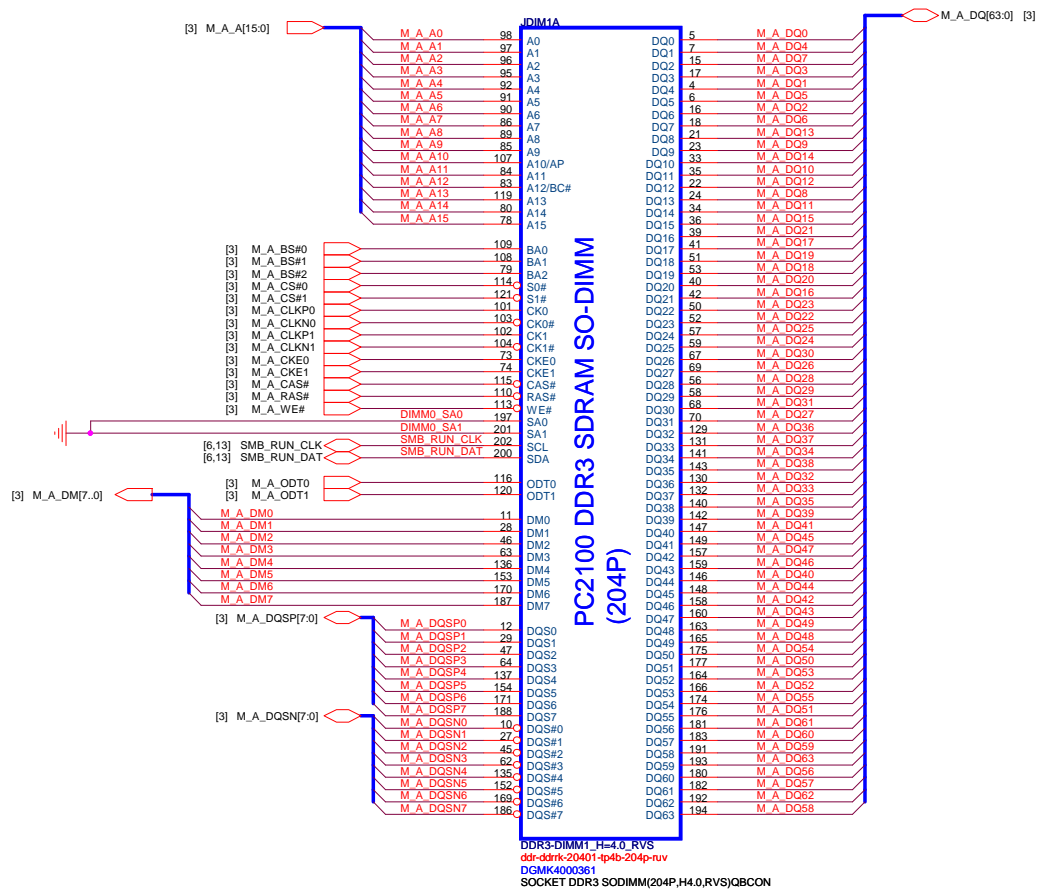
CM



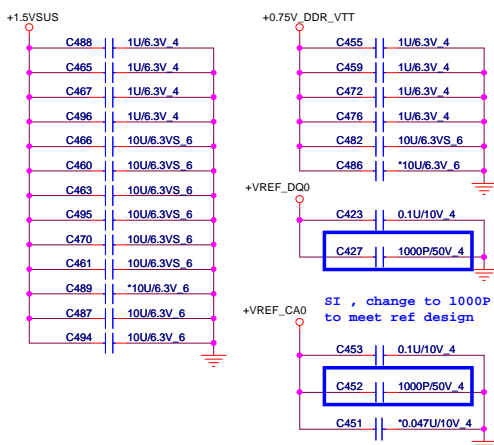
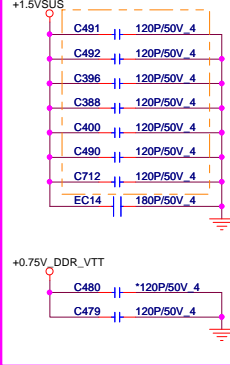
Close to Pin8



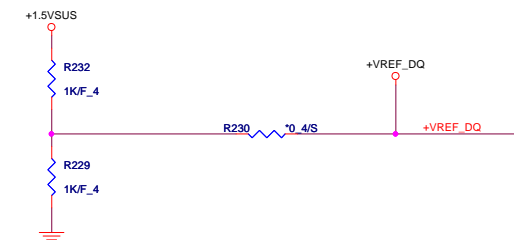
EE PROM	R3054,R3056
EC OPTION	R3055,R3057

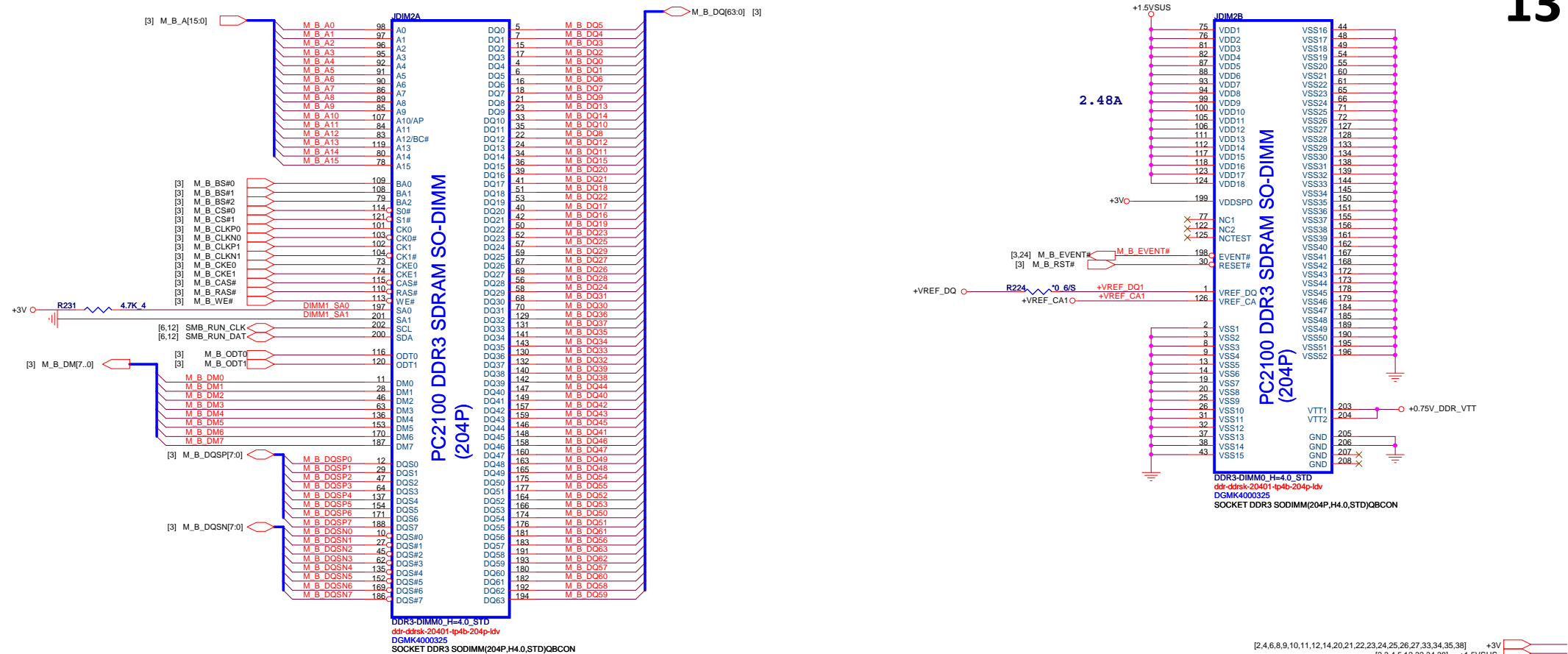


Place these Caps near So-Dimm0.

For EMI RESERVE
6/21/2012 for EMI

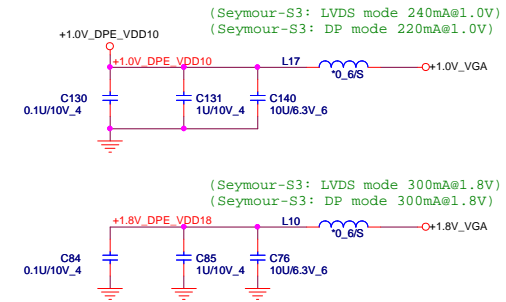
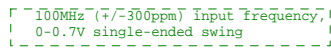
Reserved for AMD suggest



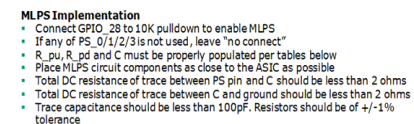


Place these Caps near So-Dimm1.

For EMI RESERVE
6/21/2012 for EMI



	Chelsea/MARS	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K

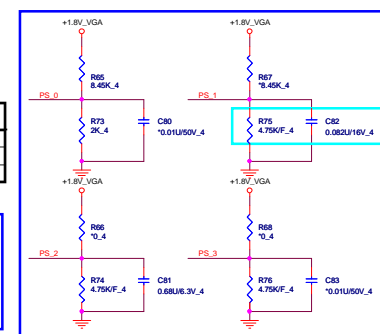


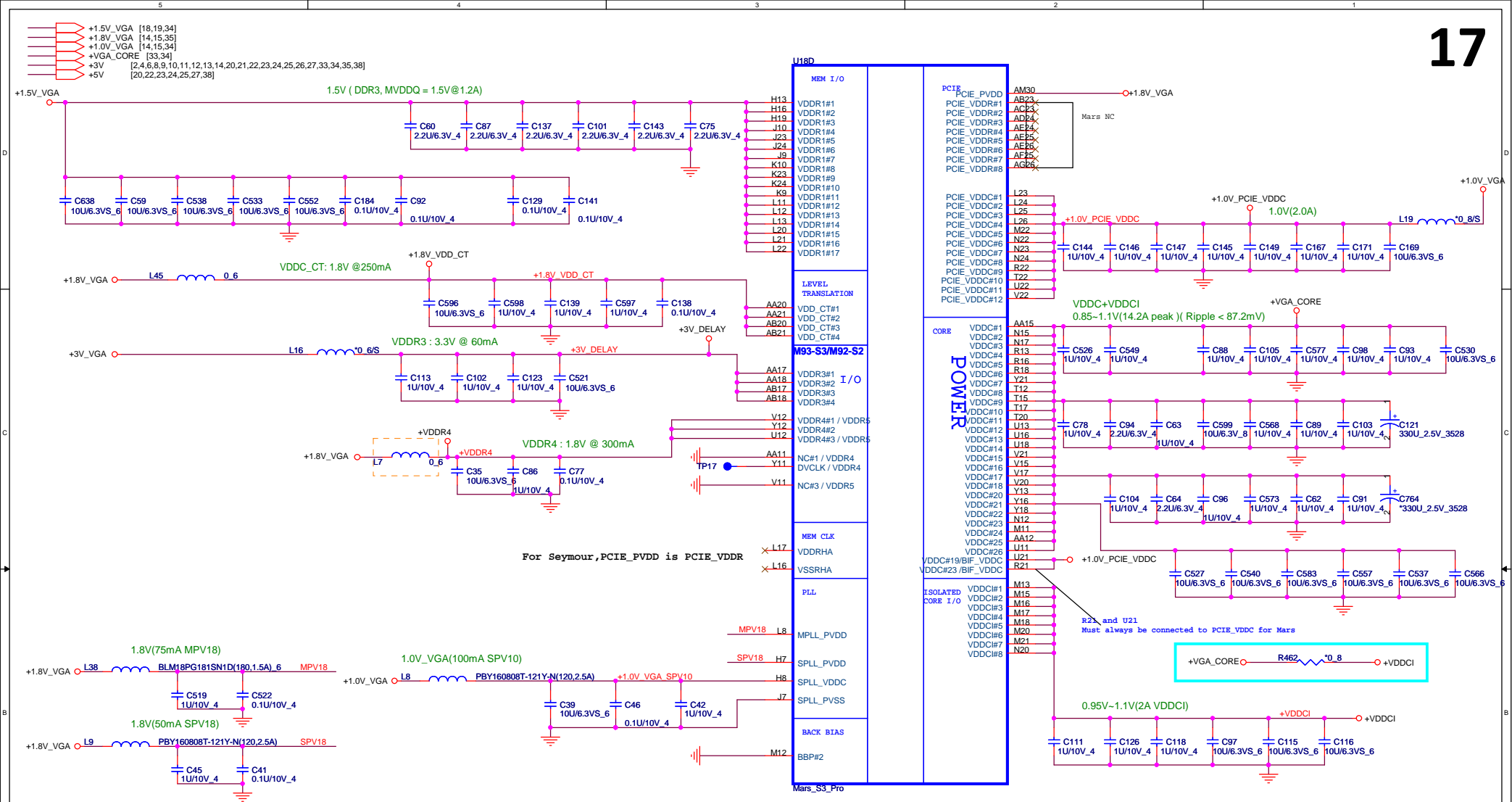
C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

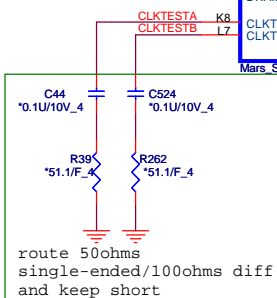
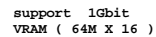
R _{pu} (Ohm)	R _{pd} (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

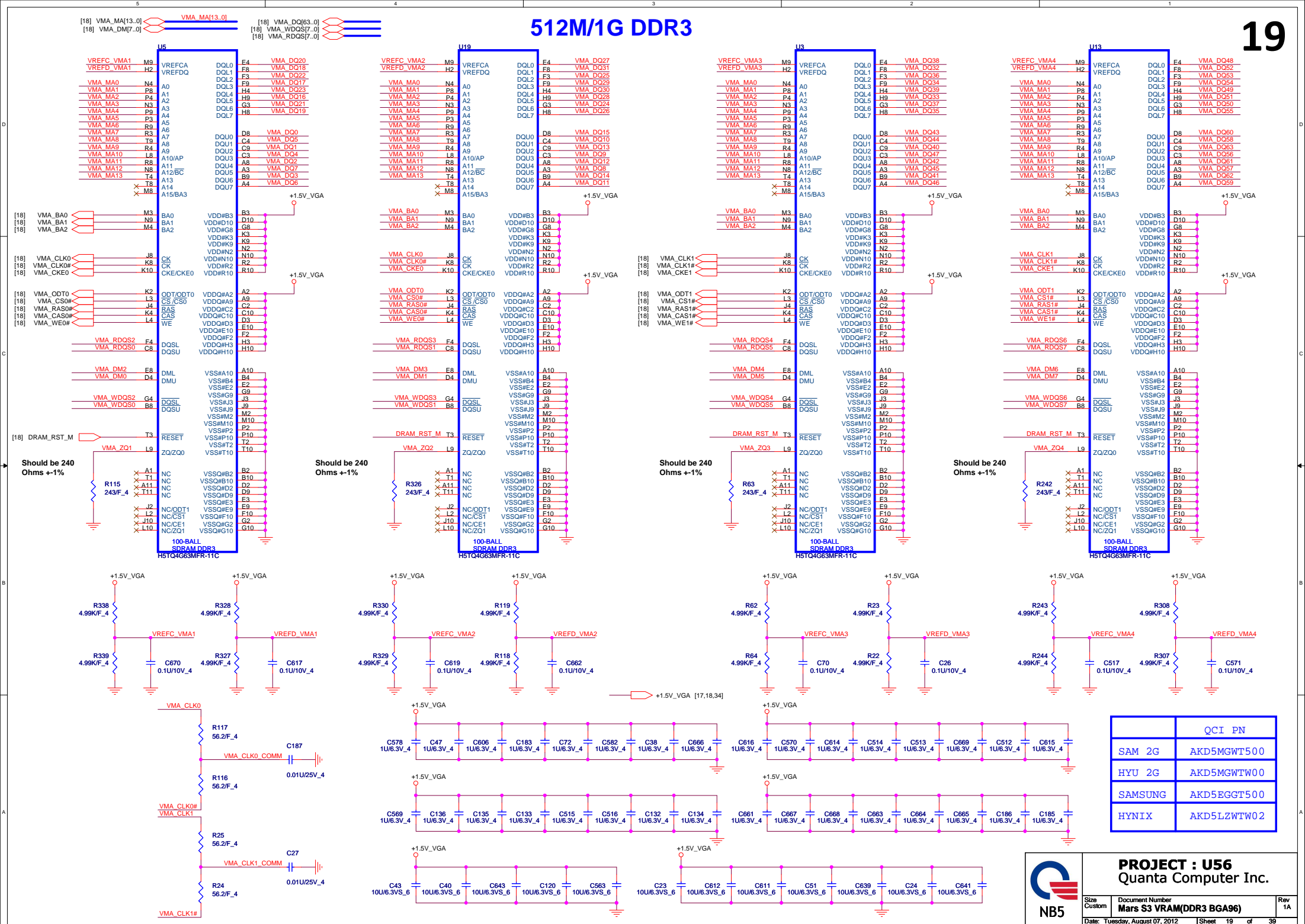
Pin/Bt	Name	Description	Default	Legacy
PS_0[3:1]	romidcrg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcrg[2:0] define memory aperture size If bios_rom_en = 1, romidcrg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genk_vsyn
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_2[2]	bif_ck_pm_en	PCIe CK PM capability: 1 = CLKREQB supported	x	gpio_8
PS_3[3]	n/a	Reserved		genk_ck
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_0[5]	aud_port_cp[0]			

BIT5 => BIT0	
PS0	=> 11001
PS1	=> 01000
PS2	=> 00000
PS3	=> 11000



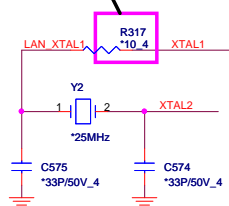






	QCI PN
SAM 2G	AKD5MGWT500
HYU 2G	AKD5MGWTW00
SAMSUNG	AKD5EGGT500
HYNIX	AKD5LZWTW02

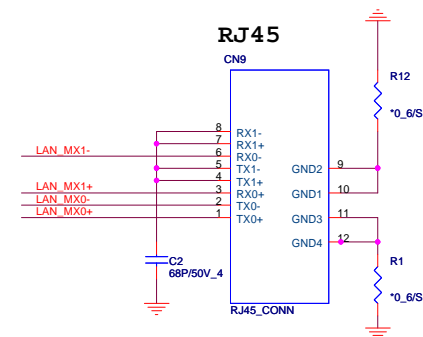
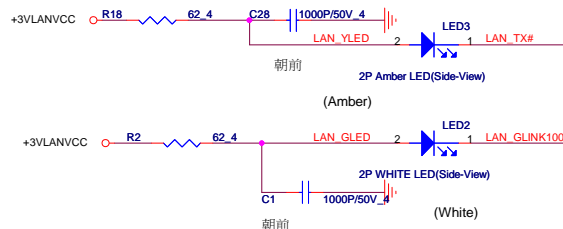
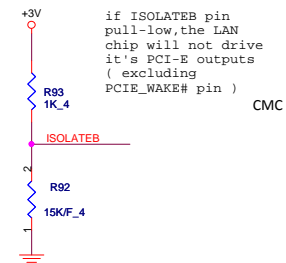
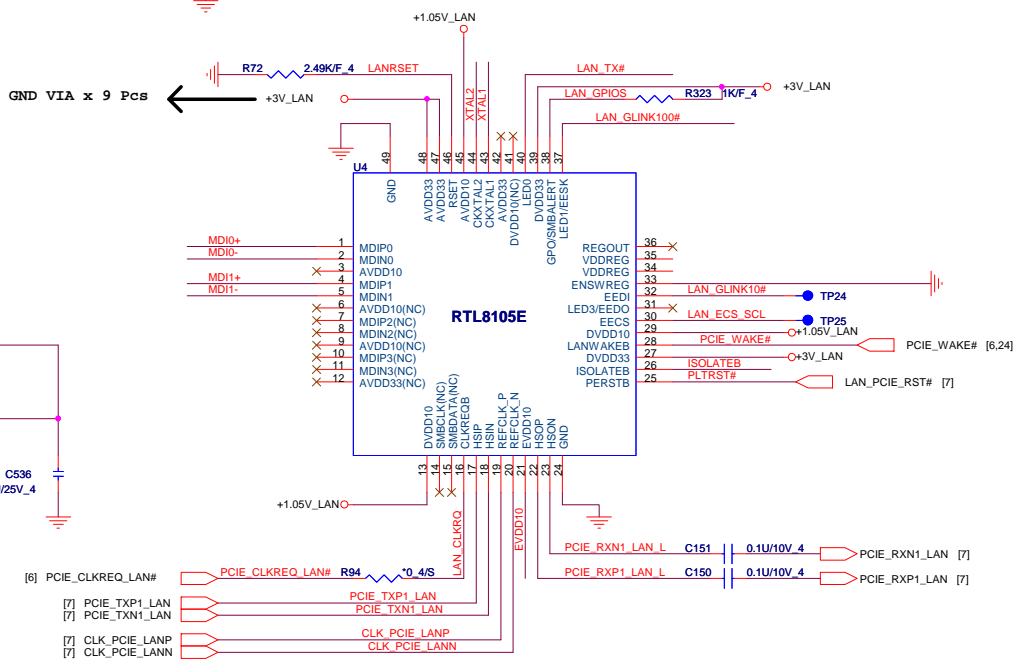
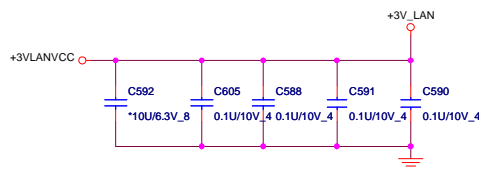
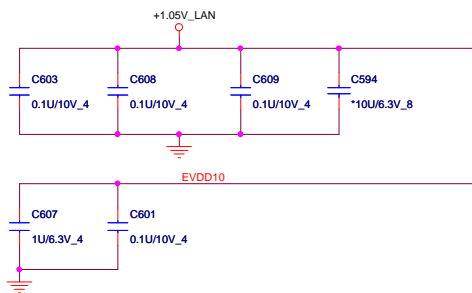
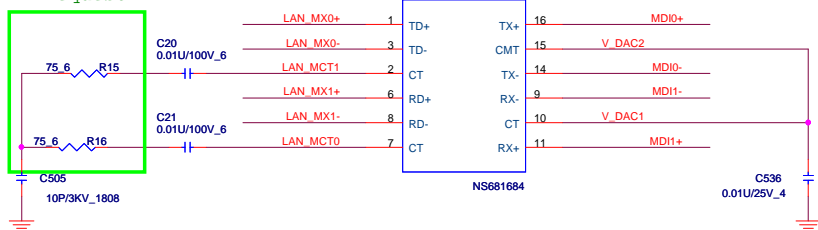
For EMI 0 ~ 22 ohm



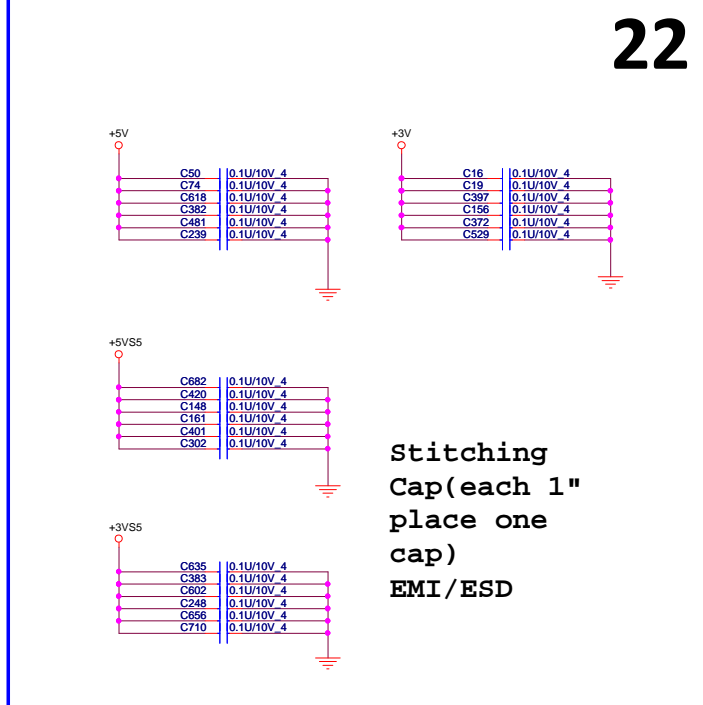
Green Clk

[24] LAN_XTAL25_IN R315 510F 4 XTAL2

Change to 0603 size for EMI request

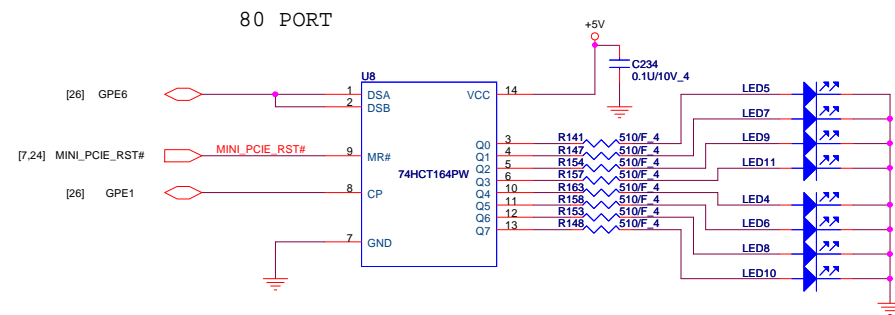
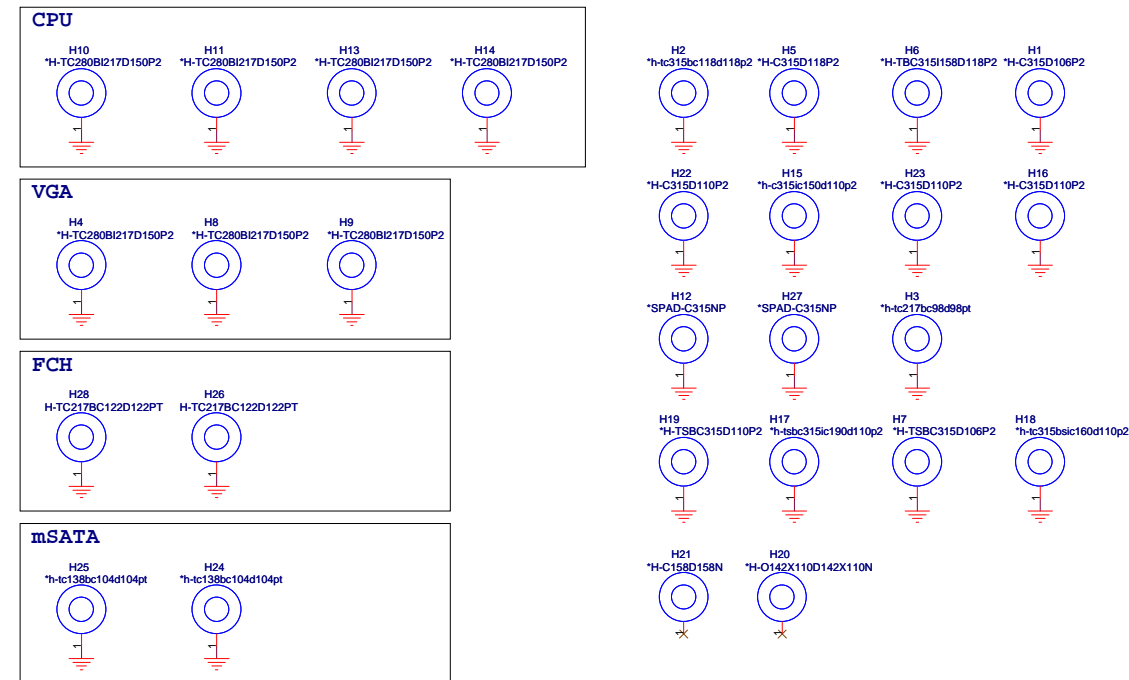


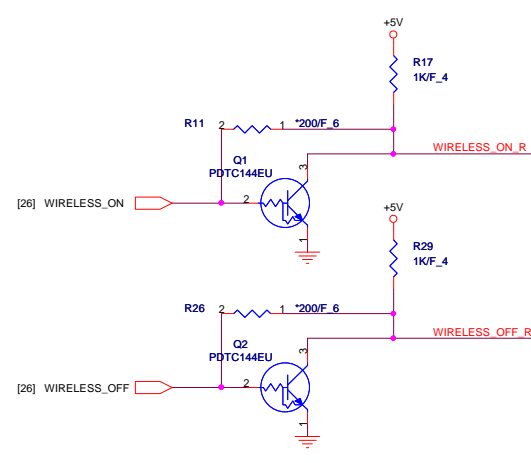
SD / MMC



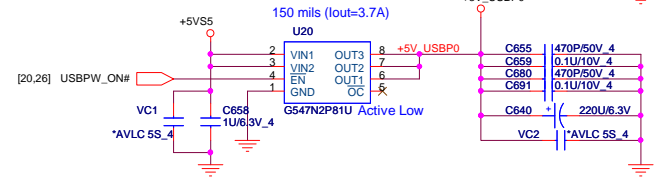
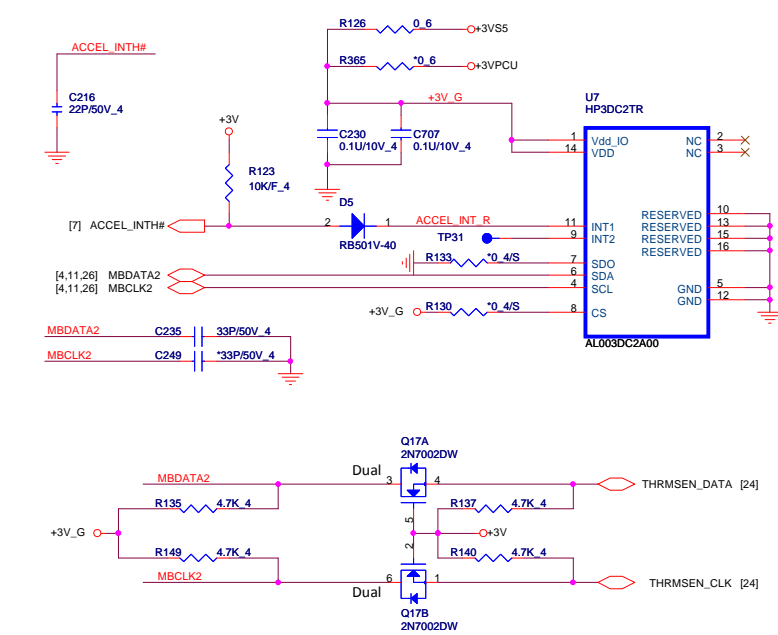
Note:

1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin1
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4

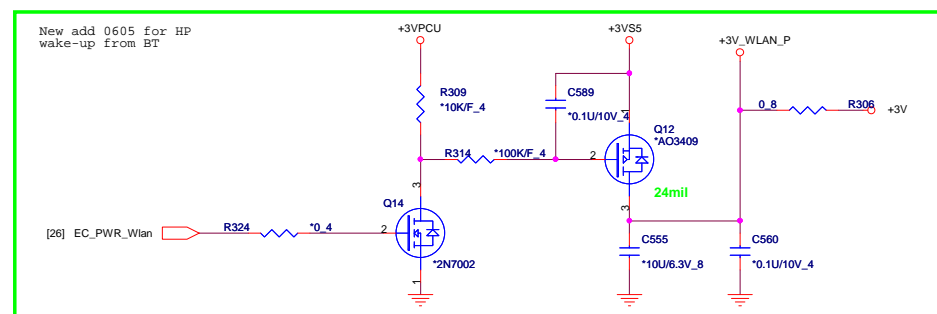
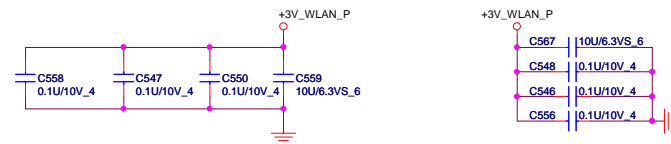
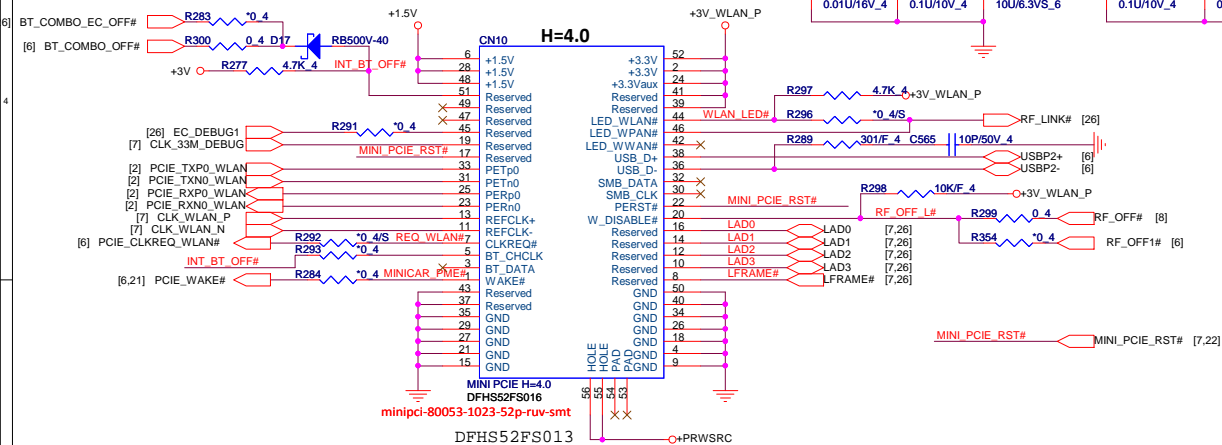




Accelerometer Sensor

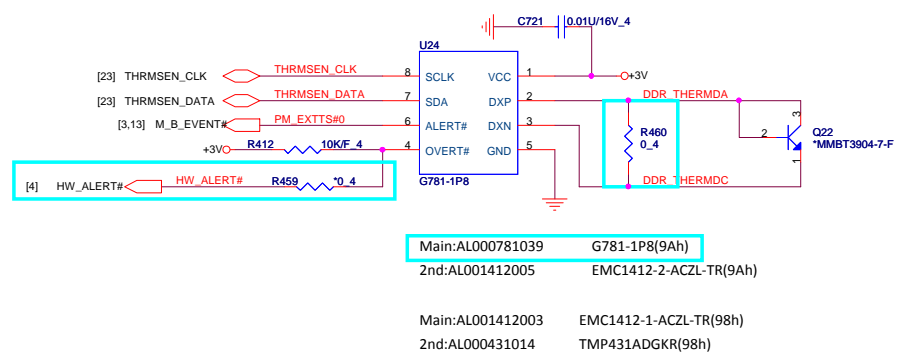


**Mini Card
WLAN/BT(Optional)**

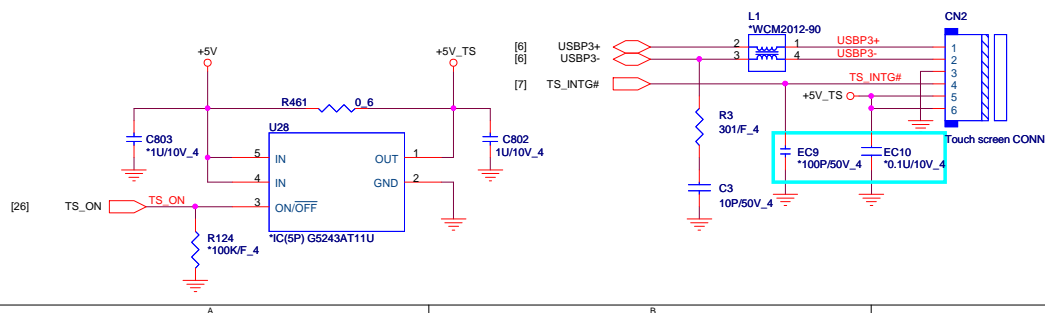


Local Thermal Sensor

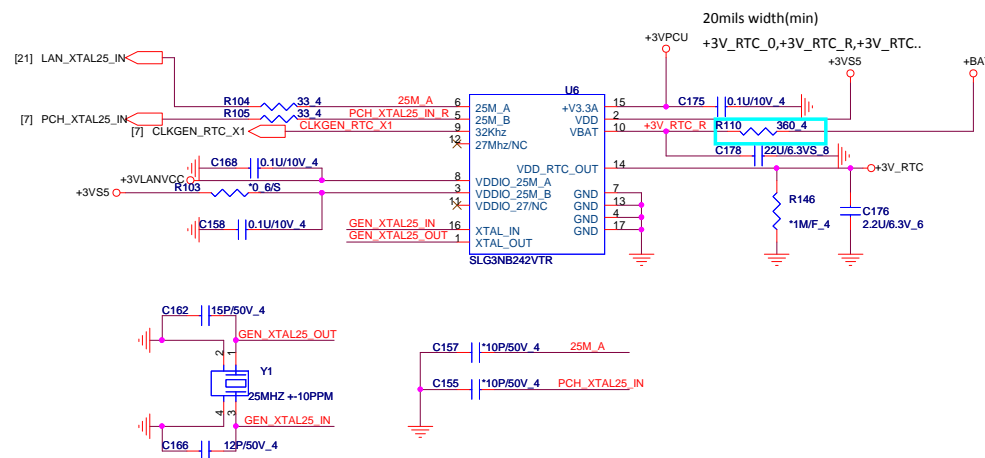
DDR3 Thermal Sensor



Touch screen

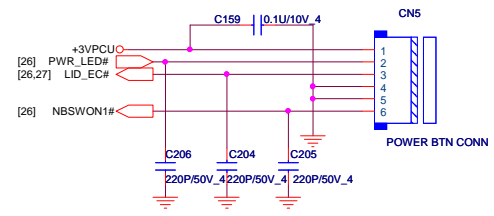


Green CLK Circuitry

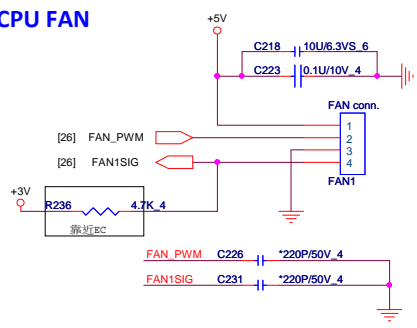


Power Button Connector

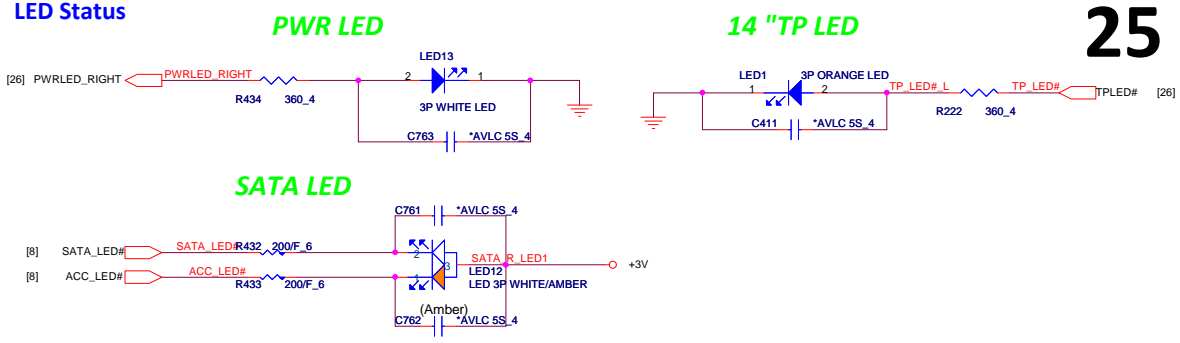
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



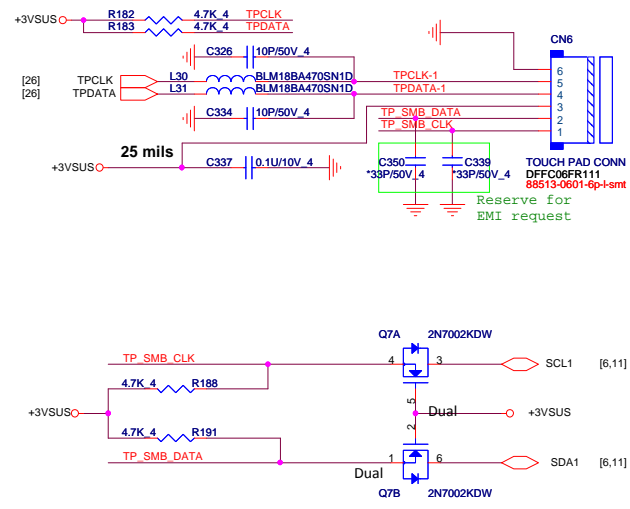
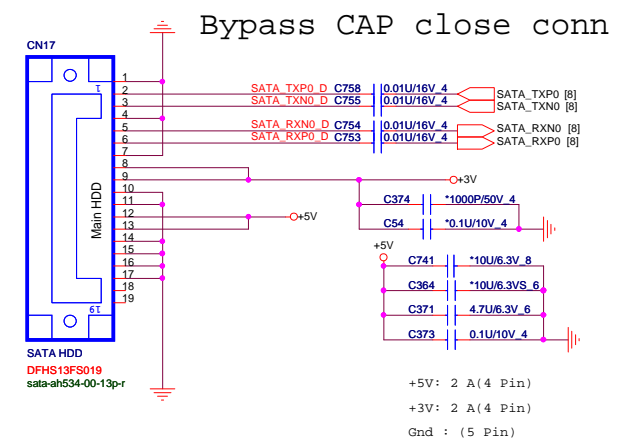
CPU FAN



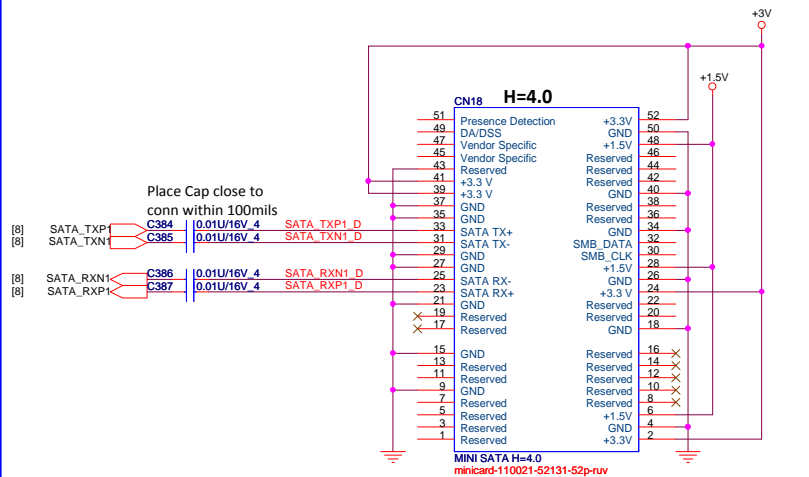
LED Status



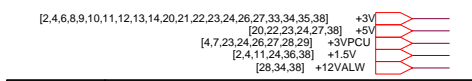
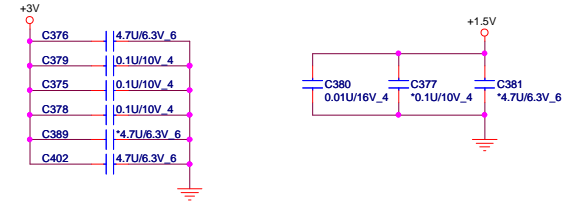
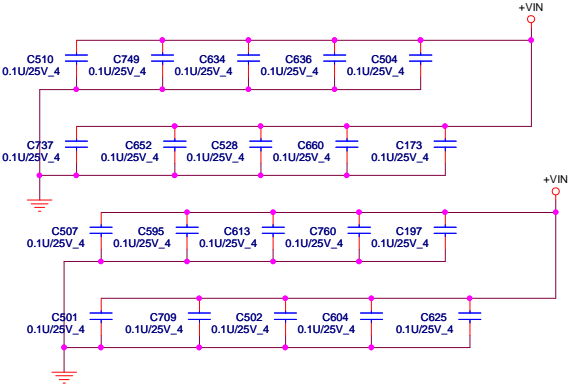
SATA HDD Connector(Cable type)

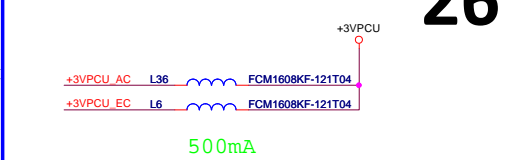


Mini PCI-E Card 2- Full size mSATA

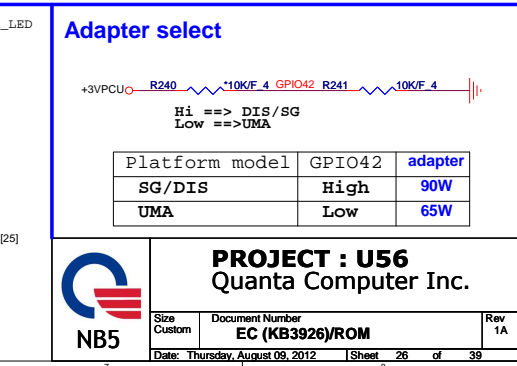
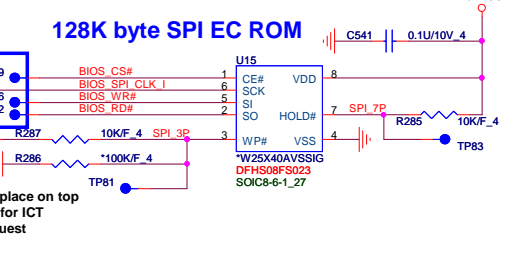
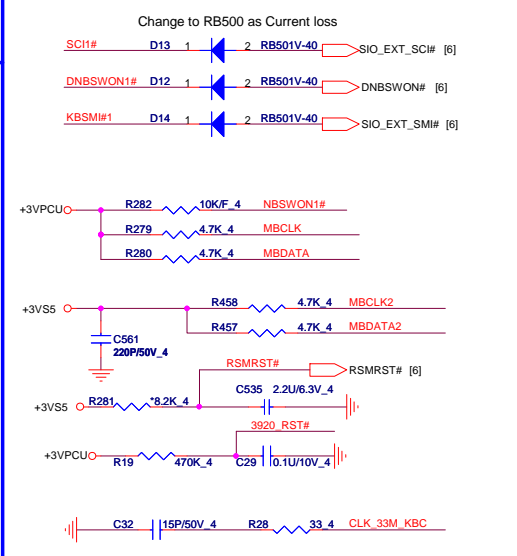


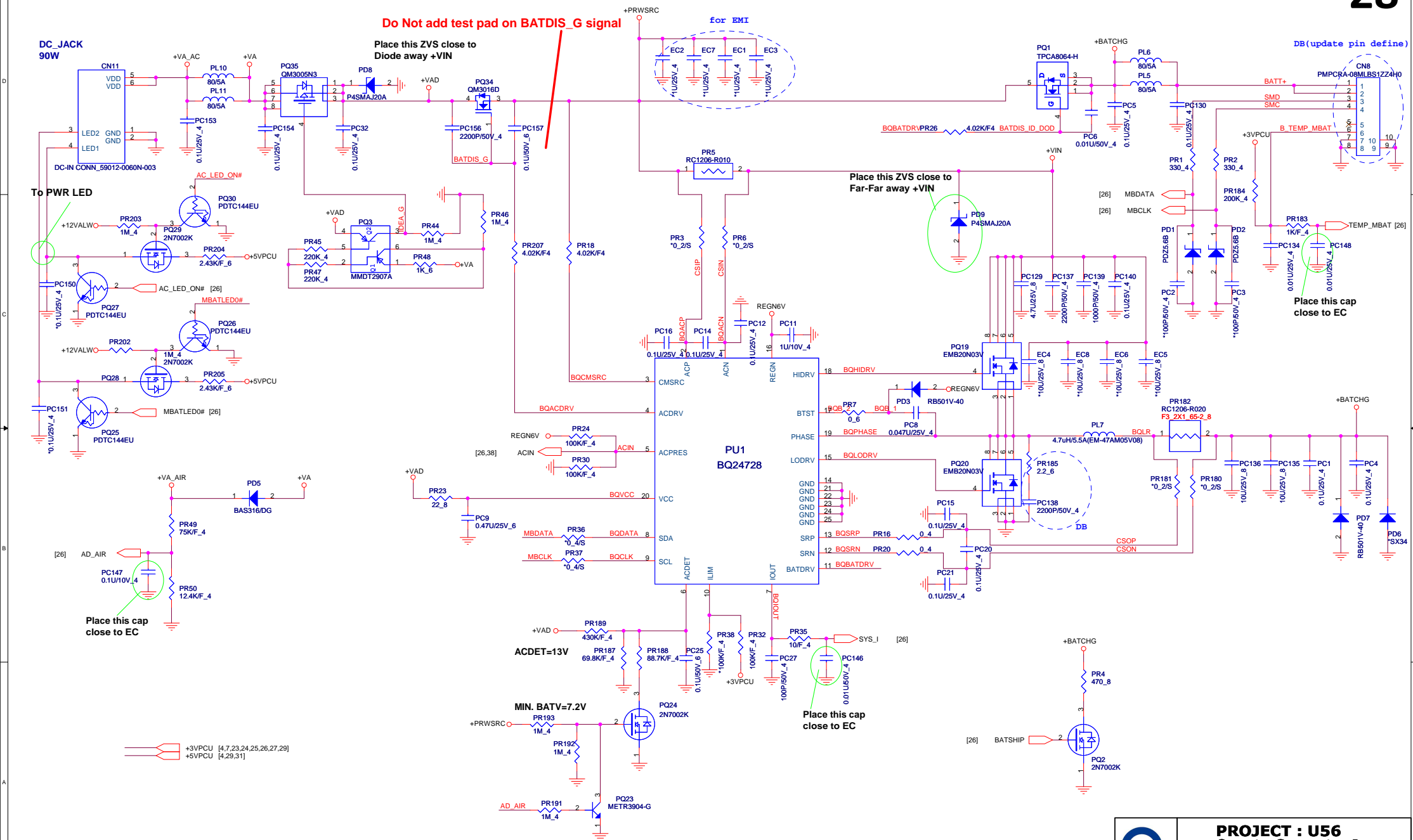
+VIN Cap





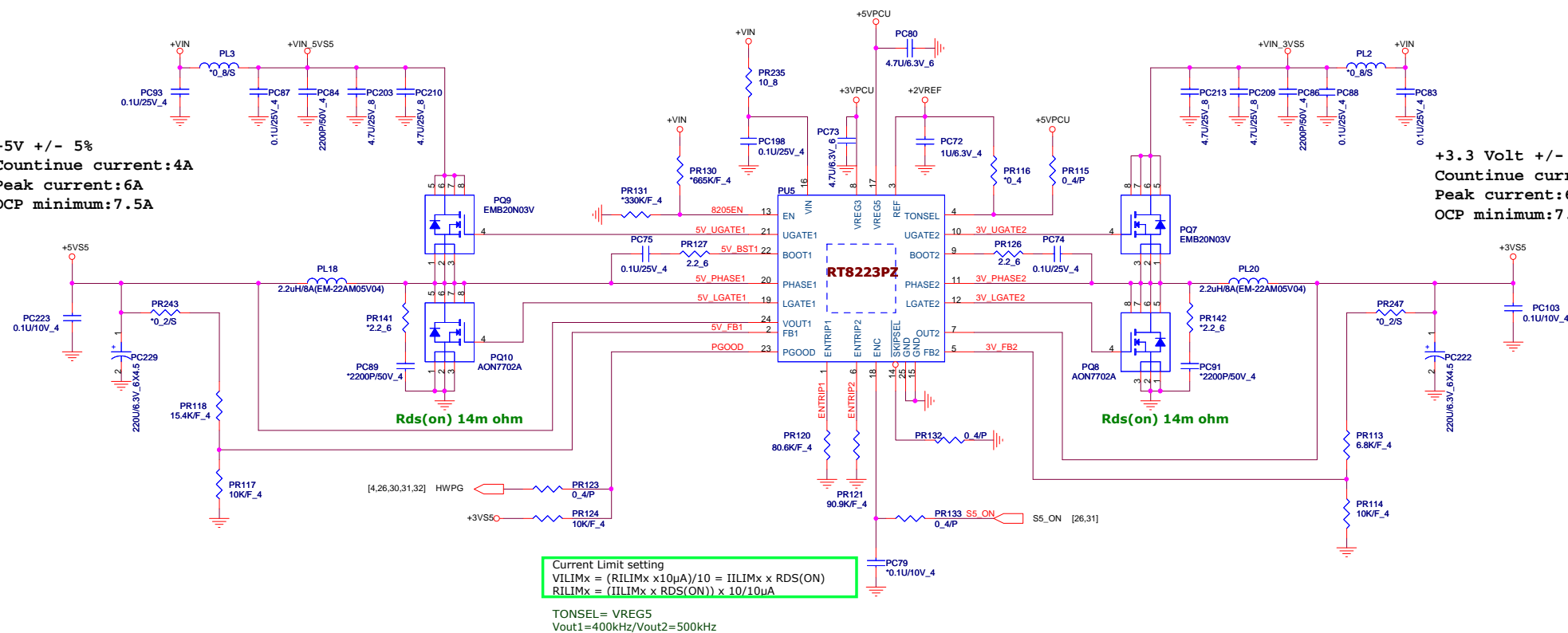
4M SPI EC ROM



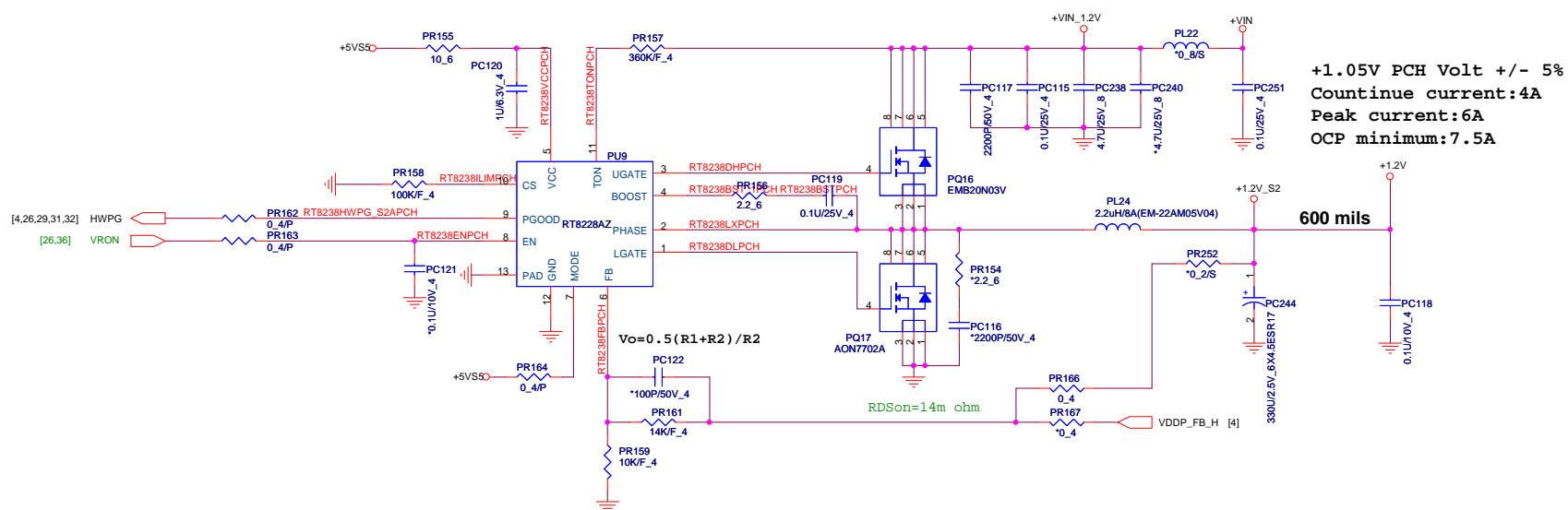


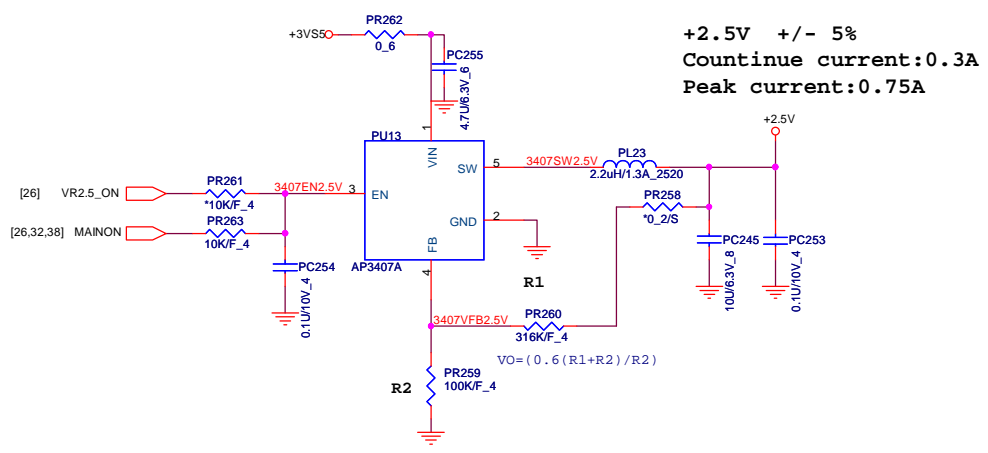
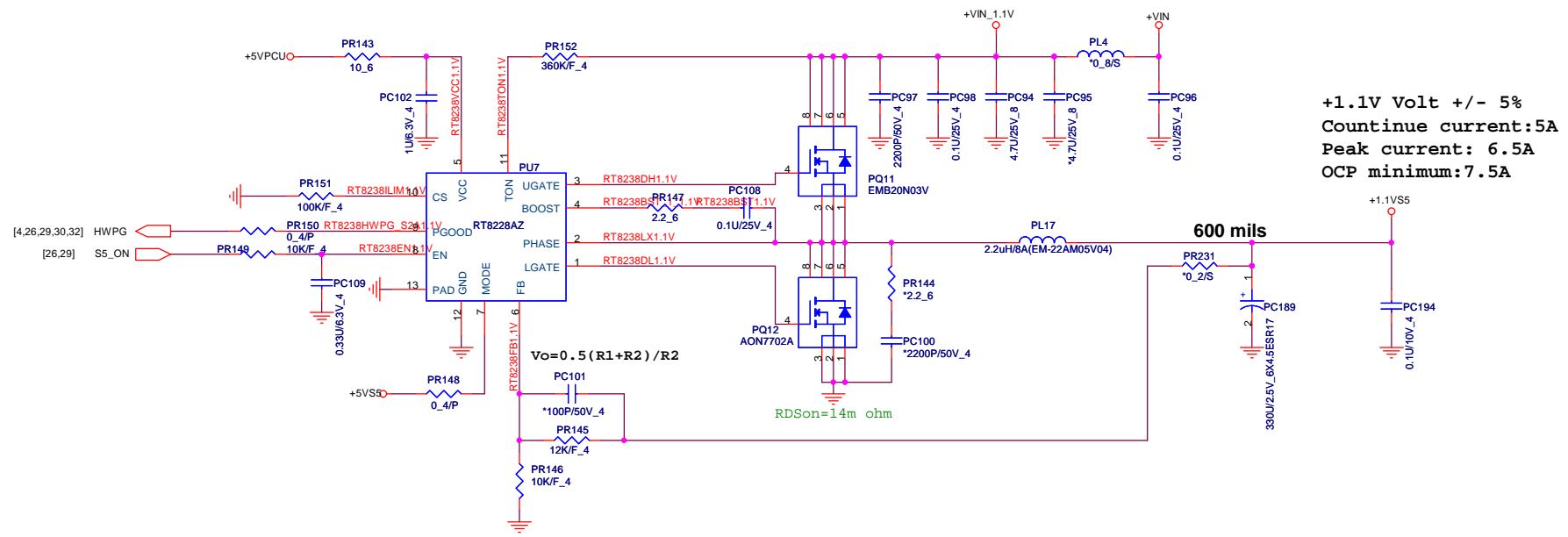
+5V +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

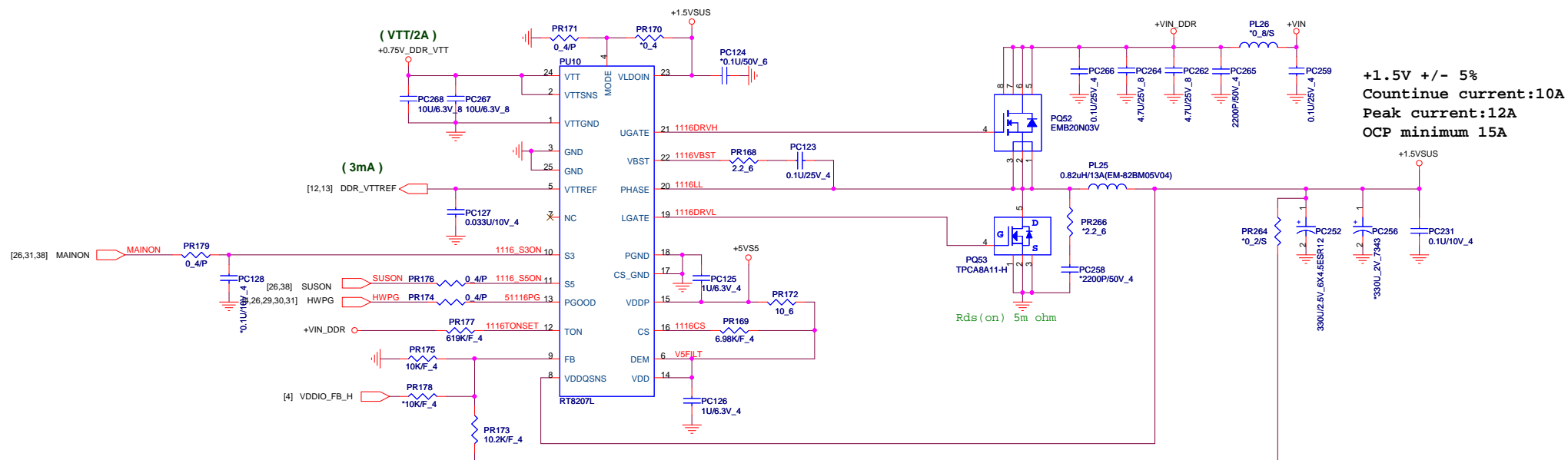
+3.3 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A



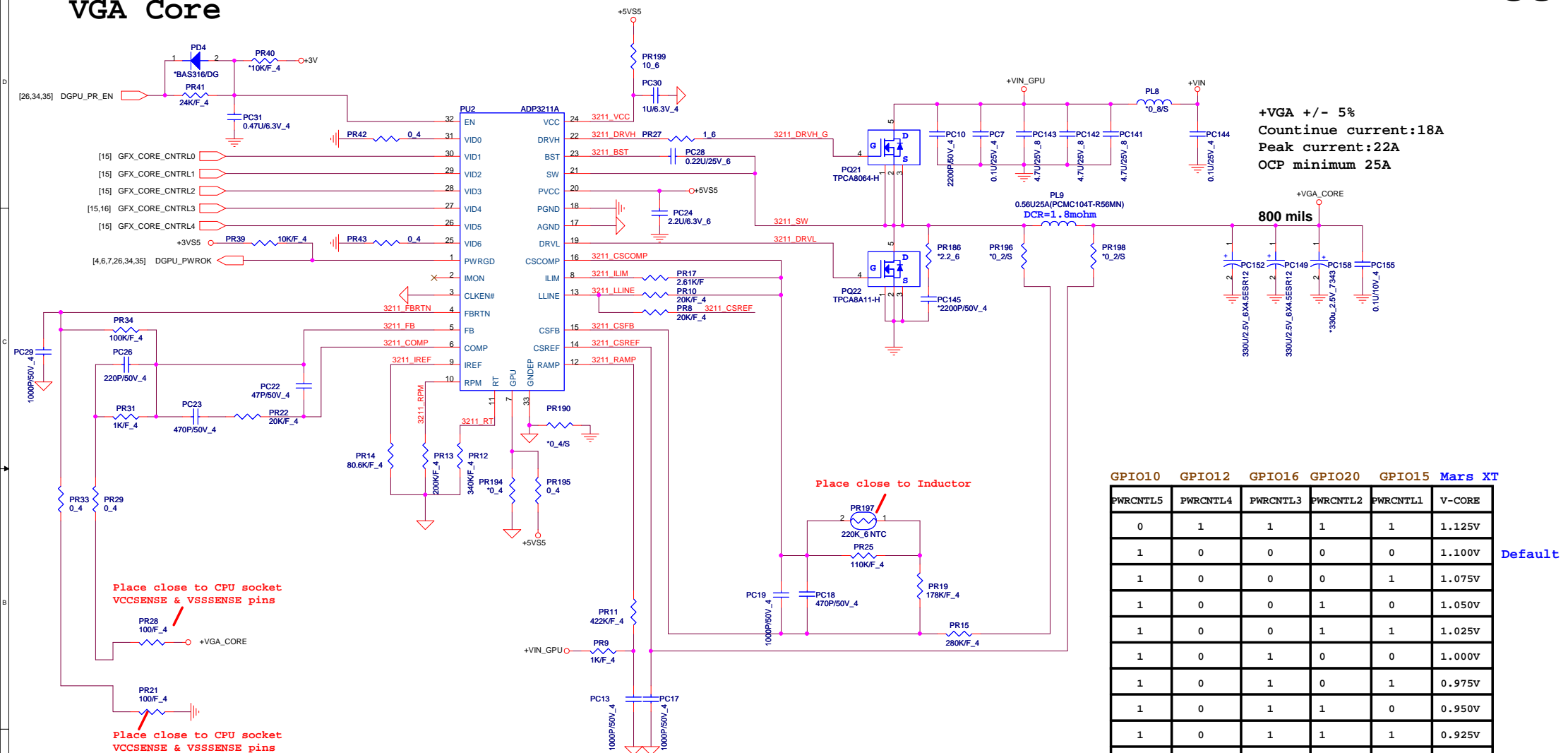
[25,27,28,30,31,32,33,34,35,37,38] +VIN
 [6,8,9,10,22,23,24,26,31,33,34,38] +3VSS
 [20,22,23,30,31,32,33,35,36,37,38] +5VSS
 [4,7,23,24,25,26,27,28] +3VPCU

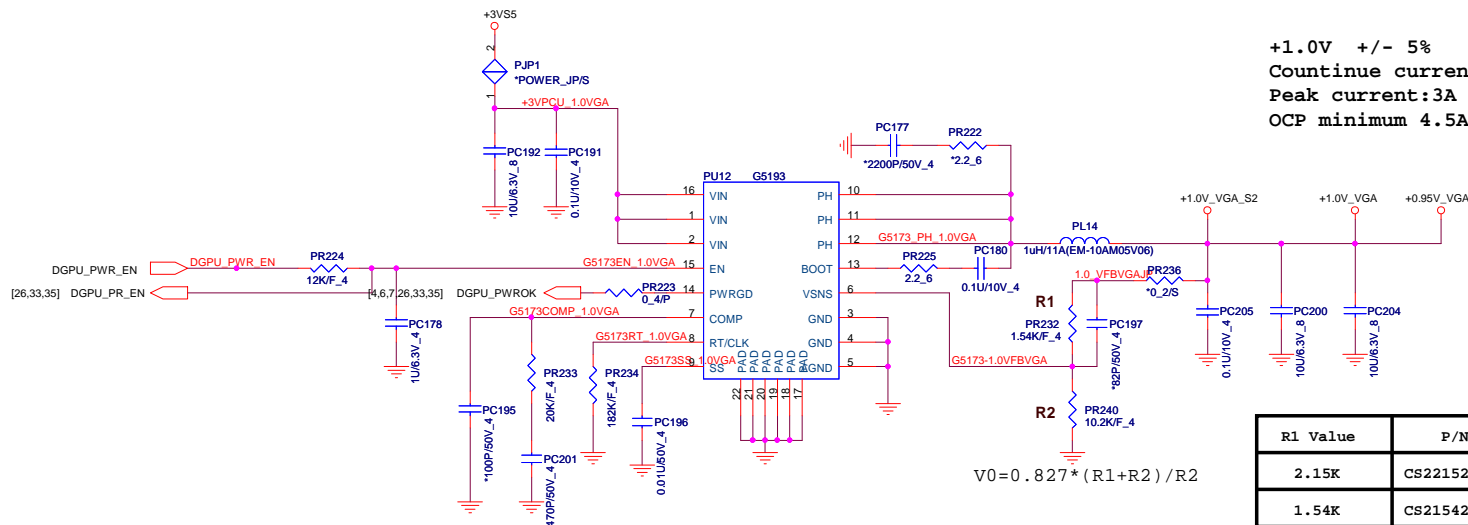




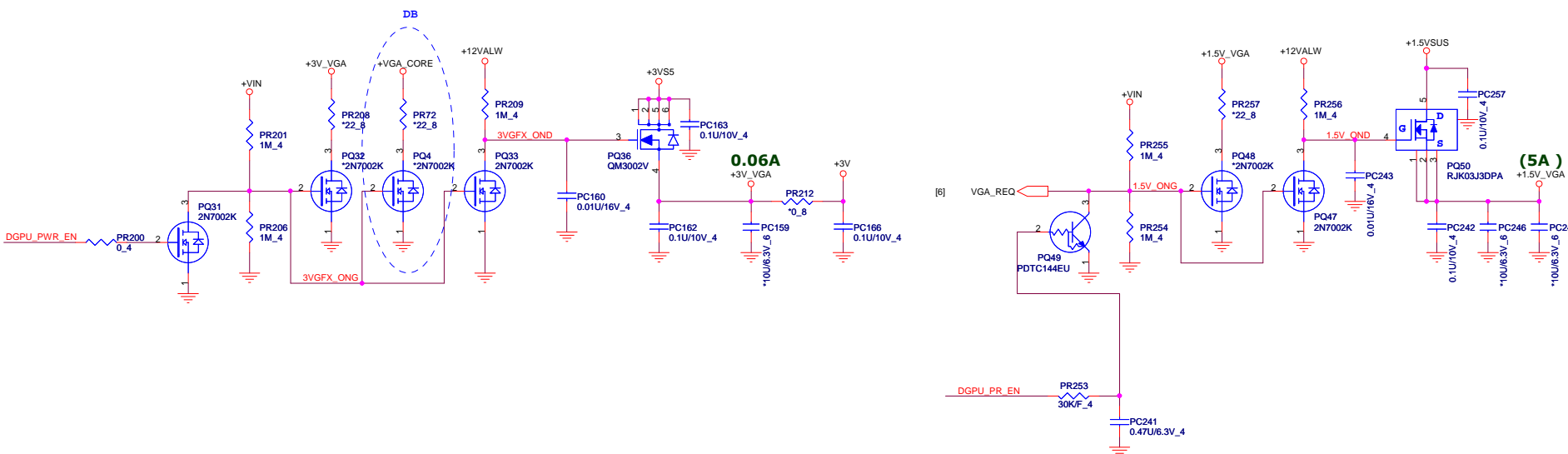
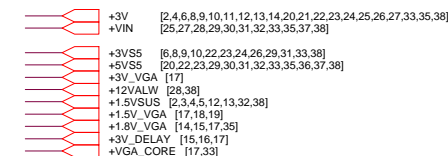


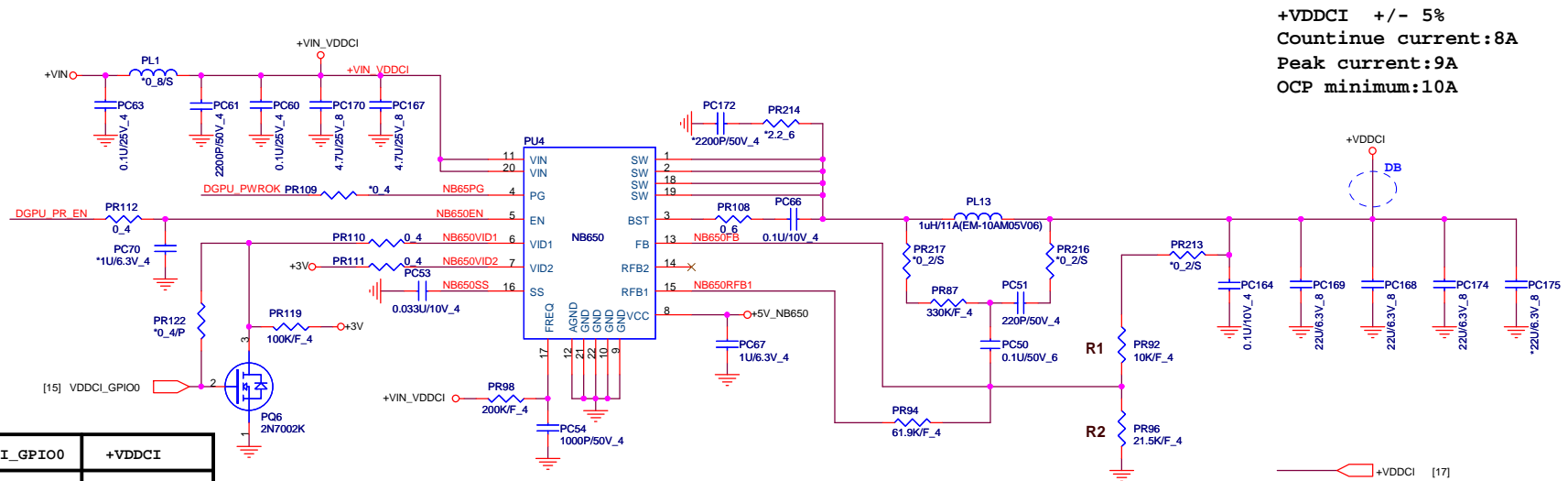
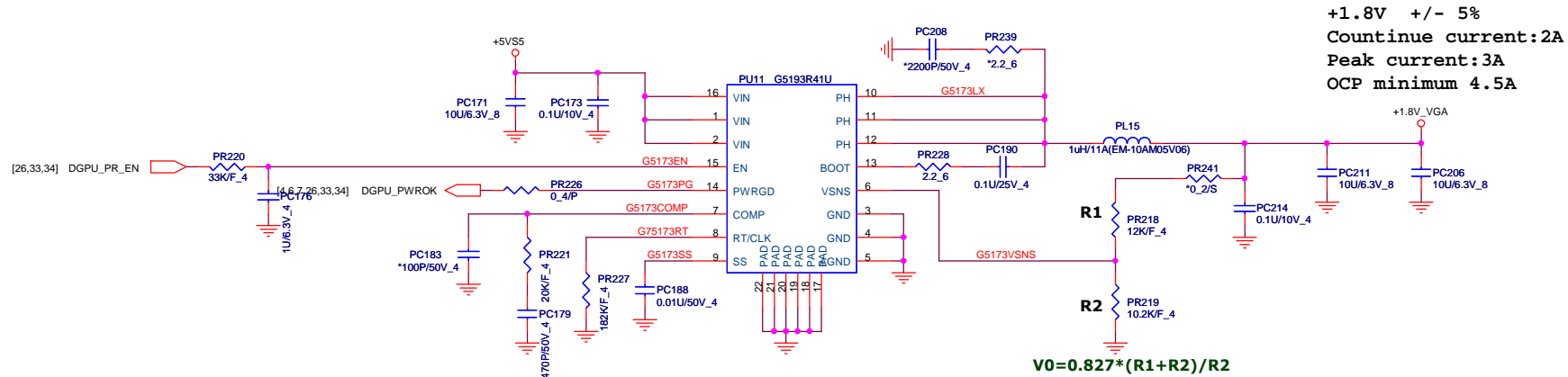
VGA Core





R1 Value	P/N	1.0V_VGA
2.15K	CS22152FB07	1.0V
1.54K	CS21542FB00	0.95V



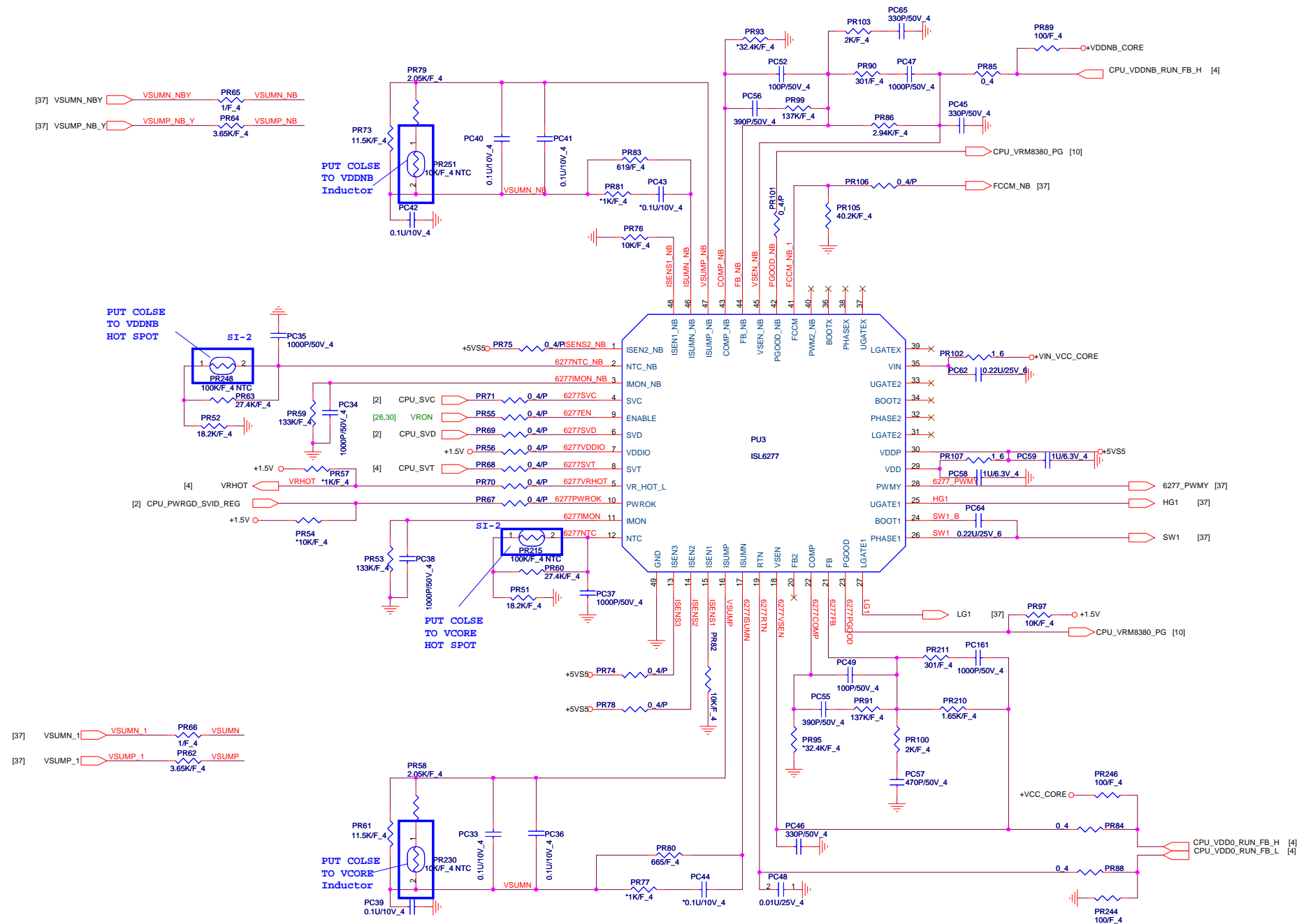


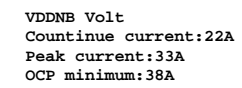
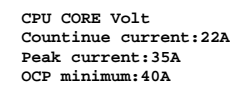
VDDCI_GPIO1	VDDCI_GPIO0	+VDDCI
X	0	1.0V
X	1	0.9V
X	X	X
X	X	X

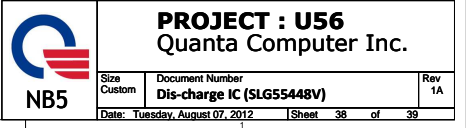


PROJECT : U56
Quanta Computer Inc.

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